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An RF-SoC-Based Ultra-Wideband Chirp Synthesizer

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ABSTRACT This paper presents the design and development of a digital two-channel chirp synthesizer using a field-programmable gate array (FPGA) device. To achieve an integrated solution, the design was implemented on radio-frequency system-on-chip (RF-SoC) technology that includes digital-to-analog converters (DACs) and other radio-frequency components on-chip. To overcome the timing errors in high-speed design with DACs operating at 6.144 GHz, a memory-stitching concept was used. A prototype was developed to validate this concept by generating a baseband chirp with a bandwidth of 1.7 GHz and a sweep time of 36 μs. The synthetic chirp was upconverted to 3.572-5.272 GHz for use as the transmit signal for an ultra-wideband radar to characterize the chirp using a 1 km long optical delay line. The transmit signal was analyzed in terms of phase and amplitude errors and corrected for these errors. The root-mean-square (RMS) frequency deviation of the predistorted chirp from linearity over the 1.7 GHz bandwidth is 9.64 kHz, realizing a chirp linearity of 0.00057%. The measurement data show comparable performance of our chirp synthesizer against a commercially available arbitrary-waveform-generator (AWG) operating at a sampling rate of 60 GHz. The reported chirp synthesizer can be used in frequency-modulated continuous-wave (FM-CW) and stretch radars. Such radars are widely used for a variety of remote sensing measurements.

INDEX TERMS RF-SoC, chirp-synthesizer, FM-CW, radar, FPGA.

I. INTRODUCTION

Ultra-Wideband (UWB) frequency-modulated continuous-wave (FM-CW) radars are widely used for airborne snow measurements over sea ice, ice sheets in Greenland and Antarctica, and land [1]–[4]. In addition, UWB FM-CW radars have been developed and used for soil moisture and other remote sensing measurements [5], [6]. UWB stretch radars are also being considered for satellite-based measurements of snow accumulation over ice sheets [7]. A major requirement for these radars is a fast and ultra-linear chirp signal.

Many UWB radars use a mixed-signal approach consisting of phase-locked loop (PLL)-based chirp synthesizers with a reference low frequency direct digital synthesizer (DDS) [8]–[13]. The fast chirp required for airborne applications results in phase nonlinearities that degrade radar performance. In addition, despite the high bandwidth capability of these methods, they lack the reconfigurability to support a wide range of applications. The UWB microwave signal for FM-CW radars can also be generated using exclusively digital methods. Methods for implementing digital chirp synthesizers were introduced as early as 1991 [14], and

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there have been many studies addressing the design of field-programmable gate array (FPGA)-based chirp synthesizers. Gomez-Garcia *et al.* generated a chirp with 750 MHz bandwidth using FPGA through a parallel DDS implementation and then employed frequency multiplication by a factor of eight to obtain a 6 GHz bandwidth [9]. Frequency multiplication of low frequency chirps results in significant phase noise degradation. The phase nonlinearity and amplitude modulation of the chirp require extensive post-processing to reduce the range sidelobes.

Chua and Koo reported an FPGA-based chirp synthesizer capable of producing a 50 MHz chirp using both DDS and memory-based methods [15]. Firmansyah and Yamaguchi developed a memory-based FPGA chirp generator operating over a 5 MHz bandwidth with 10 μs sweep time using the OpenCL framework [16]. Wang *et al.* used an improved CORDIC algorithm to design a chirp generator at 2.417 GHz with a bandwidth of 1.25 MHz [17]. Prager *et al.* reported wideband chirp synthesis using a frequency stacking method on a commercial software-defined radio (SDR) platform [18].

In this paper, we describe a digital chirp synthesizer that generates a 1.7 GHz wideband chirp. The reported chirp synthesizer uses a memory-based approach to generate fast ultra-linear chirps appropriate for ultra-wideband airborne radars for operation on both manned and unmanned aircraft. Such chirps are very useful for providing near real-time snow and soil moisture data products to support operational applications with minimal additional post-processing. The developed chirp synthesizer is implemented using Xilinx radio-frequency system-on-chip (RF-SoC) technology with integrated high-speed digital-to-analog converters (DACs) operating at a maximum sampling rate of 6.554 GSPS. The high sampling rate of the DAC can lead to timing challenges in high-speed designs. To overcome the critical timing errors, we used an FPGA-based memory-stitching method that can extend the chirp bandwidth and offer the opportunity to implement FM-CW and stretch radars based on an RF-SoC platform.

To improve the chirp linearity and point target response, the timing diagram of the system is thoroughly analyzed to avoid discontinuities between the chirp data coming from different memory elements. In the reported design, we employed central direct memory access (cDMA) method to minimize processor overhead for data transmission to DACs. To demonstrate the synthetic chirp in an operating radar, an upconversion chain was designed to shift the baseband frequency by 3072 MHz to be in the operating frequency range of an existing ultra-wideband radar at the University of Alabama. In addition, we predistorted the transmit chirp to reduce the phase errors and amplitude modulation effects to obtain a point target response close to an ideal. Furthermore, we corrected the residual radar receiver phase errors to generate an ideal point target response.

Section II briefly reviews the operating principle of an FM-CW radar. Section III describes the technical details of the chirp synthesizer that we developed, and Section IV provides the phase and amplitude error analyses and presents the radar measurement results. Finally, Section V concludes the paper.

II. FM-CW RADAR PRINCIPLE

In an FM-CW radar, the transmitted chirp signal frequency is increased or decreased linearly over the desired bandwidth, B, within the sweep time of T and can be expressed as follows:

$$s(t) = e^{j2\pi(f_0 t + \frac{\alpha}{2}t^2)} \tag{1}$$

where $\alpha = \frac{B}{T}$ and $0 \leq t \leq T$. In a typical FW-CW radar, the received signal is mixed with a sample of the transmitted signal to obtain a beat frequency proportional to the target range. The beat frequency for the sawtooth chirp is given by:

$$f_b = \alpha\tau = \frac{B}{T}\frac{2R}{c} \tag{2}$$

where f_b is the beat frequency in Hz, B is the transmitted chirp bandwidth in Hz, T is the chirp sweep time in seconds, R is the target range in meters, and c is the propagation velocity of the transmitted wave in m/s.

III. RESEARCH METHODOLOGY

A digital chirp synthesizer was developed using a Xilinx ZCU111 RF-SoC development board [19], as shown in Figure 1. In addition to the FPGA fabric, the RF-SoC is equipped with eight integrated high-speed 14-bit 6.544 GSPS DACs and a quad-core Arm Cortex A53 processor. Using this RF-SoC to design a high-speed memory-based chirp synthesizer is challenging because of limited memory storage on the FPGA fabric and critical timing requirements. As the memory blocks are distributed across the RF-SoC chip, a higher memory size results in larger interconnect propagation delay throughout the FPGA fabric, leading to unresolvable timing errors. Therefore, a memory-stitching concept is introduced to overcome critical timing requirements.

Four identical block-random-access-memories (BRAMs) were used to develop the proposed chirp synthesizer. As the total number of cells in each of the instantiated BRAMs is equal, a unique address counter can be utilized to loop through the cells of each BRAM simultaneously. Chirp data were generated using MATLAB and then quantized for conversion to a binary data file. We used the PYNQ framework to develop a driver application for the RF-SoC. A detailed review of this framework is provided in [20]. On chip level, chirp data are first stored in processor double-data-rate-4 (DDR4) memory and then transferred into BRAMs on FPGA fabric through a central DMA system. Each BRAM has its own controller, which is managed by central DMA, as shown in Figure 1. All subsystem communications between FPGA fabric and processor system occur through the AXI interconnect based on a 100 MHz pl_clk provided by the ZYNQ UltraScale+ processor intellectual-property (IP) core. However, the data converter IP has a separate clocking mechanism that feeds the rest of the system on FPGA fabric to ensure that the chirp data packets propagate synchronously

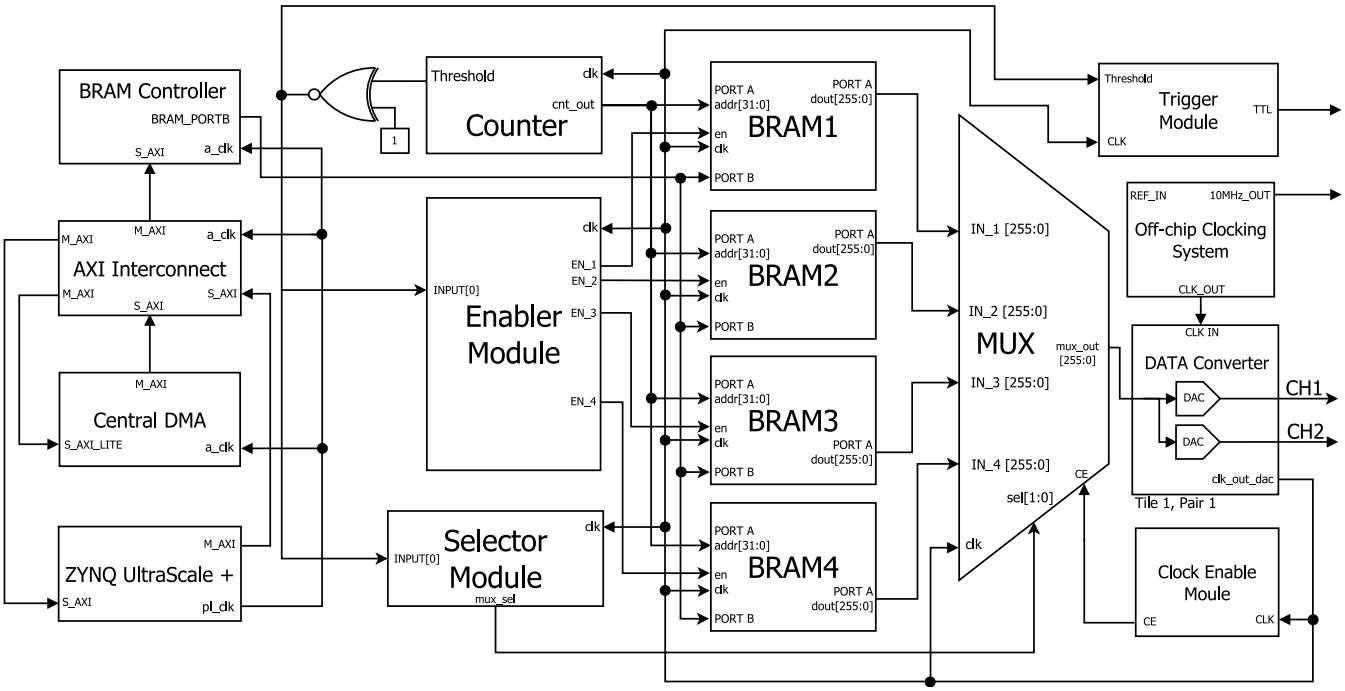


FIGURE 1. **Proposed memory-stitching architecture for multi-channel wideband chirp synthesis using RF-SoC technology.**

with the DAC clock. In the utilized XCZU28DR RF-SoC, there are two DAC tiles, each including two pairs of DACs. In this paper, only one pair of DACs was used to develop the two-channel chirp synthesizer. The clock to both tiles is supplied by LMX2595 wideband synthesizer, which is part of a complex off-chip clocking system. Further details on the ZCU111 clocking architecture are provided in [21]. In the reported chirp synthesizer, the DACs were configured to operate at a sampling rate of 6.144 GSPS. Because there are two pairs of DACs in each tile that are fed by the same clock source, they are synchronous with each other. However, to synchronize the output chirps with external systems, such as radars, a *Trigger* module was designed to assert a Transistor-Transistor Logic (TTL) signal with the activation of the first BRAM. This triggering is based on the result of the XNOR gate.

The chirp data were divided equally into four sections for downloading into each of the BRAMs, as shown in Figure 2. These data were stored in packets of 256 bits, each including 16 samples of a full-length chirp. We first assume that there are N data packets in each of the BRAMs, $P_0, \ldots, P_{N-2}, P_{N-1}$, where P_0 is the first packet and P_{N-1} is the *Nth* packet of each subpulse. Each data packet contains 16 samples of a subpulse, $S_0, \ldots, S_{14}, S_{15}$, where S_0 is the first sample and S_{15} is the sixteenth sample. An unwrapped sample from a data packet is shown in Figure 2. The first two most significant bits (MSBs) of a sample packet are zero because of the 14-bit DAC resolution. As the implemented BRAMs are byte-addressable, each sample occupies two memory addresses. Because each data packet includes 16 samples, there are 256 bits of data occupy 32 memory addresses. Thus, for proper data fetching from the BRAMs in each clock cycle, the address counter increments by 32 or 0×20.

The system clock (*CLK*) speed can be calculated by dividing the desired DAC sampling rate by the total number of samples on the data stream path, which, in this case, results in 384 MHz. As shown in the timing diagram in Figure 3, the address counter, *cnt_out* triggers the assertion of the *Threshold* signal whenever the *Counter* reaches the maximum value. At the falling edge of the *Threshold* signal, the *Enabler* module synchronously enables/disables each BRAM. In the proposed architecture, an equivalence gate, XNOR, is utilized to compare the *Threshold* value against an always high constant to generate control signals for the *Enabler* and *Selector* modules. In the *Enabler* module, the output of the XNOR gate is scanned, and if it is a high signal, the appropriate signal for enabling the next BRAM is generated. The *Enabler* module is a circular shift register that sequentially enables BRAMs through *EN*_1 to *EN*_4 signals by shifting the initial value of b0001 whenever the *Counter* reaches the maximum value. To transmit chirp samples from the four BRAMs through the DAC, a *multiplexer* module was designed. The word length of the input signals *IN*_1 to *IN*_4 of the multiplexer is proportional to the DAC data stream length, which is 256 bits. In each clock cycle, a data packet is placed on the data stream path through *mux_out*.

As the *Counter* module is piped, there are 4-clock cycles of latency until the address counter starts counting upwards from zero. At system start-up, as *Counter*, *Enabler*, and *Selector*

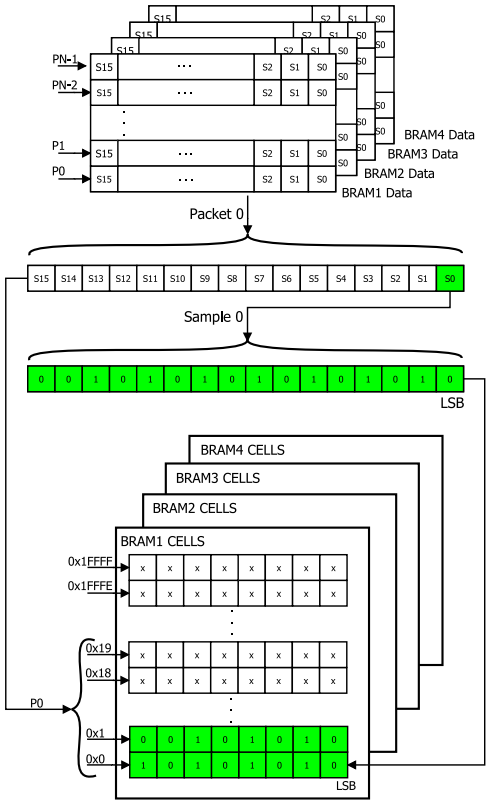


FIGURE 2. Unwrapped data packets and their distribution across memory.

modules hold initial values, the first data packet, P_0, from the first BRAM, would be placed on the data stream path through *IN*_1 for a few more clock cycles than the other samples. This causes disorganization in overall streaming, which is addressed in the next section. To avoid this issue and place data packets onto the streaming path for only one clock cycle, a *ClockEnable* module was designed and added to the system architecture. This compensates for the initial condition of the counter by allowing the multiplexer to propagate data after waiting for four clock cycles. As the output of *Selector* module, *mux_sel*, is updated at the falling edge of the *Threshold*, one clock cycle latency is added to the *Selector* module. This ensures that inputs of multiplexer are switched only when all data packets from each of the BRAMs are passed through *mux_out*, as shown in Figure 3; otherwise, data packet loss would be expected, which will result in discontinuity between the chirp data.

IV. RESULTS AND DISCUSSION

Experiments showed that any discontinuity between the data packets of BRAMs would result in high-range sidelobes. To synthesize a continuous ultra-wideband chirp from subpulses, $s(t)$ must be a continuous chirp signal, as defined in Equation (1). Using Euler's equation, $s(t)$ can be expressed as:

$$s(t) = cos(2\pi(f_0 t + \frac{\alpha}{2}t^2)) + jsin(2\pi(f_0 t + \frac{\alpha}{2}t^2) \quad (3)$$

where the second term is zero and Equation (3) can be rewritten as:

$$s(t) = cos(2\pi(f_0 t + \frac{\alpha}{2}t^2)) \quad (4)$$

where $\alpha = B/T = (f_1 - f_0)/T$ as defined in Equation (1). Equation (4) can be rewritten in discrete signal form as:

$$s[n] = cos(2\pi[f_0 n + \frac{f_1 - f_0}{2(N-1)}n^2]) \quad (5)$$

Each discrete chirp signal sweeps from f_0 to f_1 with the total number of samples equal to N, where $0 \leq n < N - 1$. Equation (5) represents a periodic waveform as:

$$s[n + kN] = s[n] \quad (6)$$

where $k = 1, 2, 3, 4, \ldots, m$. As shown in Figure 4, the discrete samples are overlapped on top of each other, indicating that Equation (6) holds true for Equation (5). We assume that n is equal to $n_1 + n_2 + n_3 + n_4$. Because the system is linear, according to the additive property, Equation (5) can be synthesized by adding multiple subpulses as follows:

$$s[n_1] + s[n_2] + s[n_3] + s[n_4] = s[n_1 + n_2 + n_3 + n_4] \quad (7)$$

Equation (7) can then be reconstructed as:

$$s[n_1] + s[n_2] + s[n_3] + s[n_4] = s[n] \quad (8)$$

Equations (8) and (6) indicate that the synthesis of an integrated chirp from multiple subpulses can be achieved by consecutively transmitting the samples from each subpulse without any delay or overlap. Discontinuities between samples would result in additional nonlinearity in the chirp spectrum.

Table 1 lists the resource utilization of the system implemented on the XCZU28DR RF-SoC chip. It can be observed that resource utilization of the reported chirp synthesizer on FPGA fabric is low. Resource utilization can be minimized by saving chip area and having faster critical path timing [22]. Optimized HDL programming is a key step in balancing FPGA resource utilization and chip area usage. In the proposed design, we addressed chip area usage and critical path improvement by utilizing multi-BRAM tiles and pipe-lining the signal path. In addition, the overall on-chip power consumption was 3.414 W. However, 2.297 W of the total power consumption is related to the quad-core Arm Cortex A53. Figure 5 shows the breakdown of the power consumption in our design. As shown, a large portion of the power consumption belongs to the ARM processor on the XCZU28DR RFSoC chip. The amount of consumed power by the logic segments and BRAM blocks is listed in Table 1.

To evaluate the proposed chirp synthesizer in a real radar system, a measurement test bench was set up, as shown in Figure 6. As the UWB radar in this setup operates from 2.7-10.7 GHz, a baseband chirp from 500-2200 MHz was synthesized and upconverted to 3.572-5.272 GHz. For this purpose, a local oscillator (LO) signal of 3072 MHz was generated from the off-chip clocking system and supplied to the LO port of the mixer. A pair of low-pass filters (LPF)

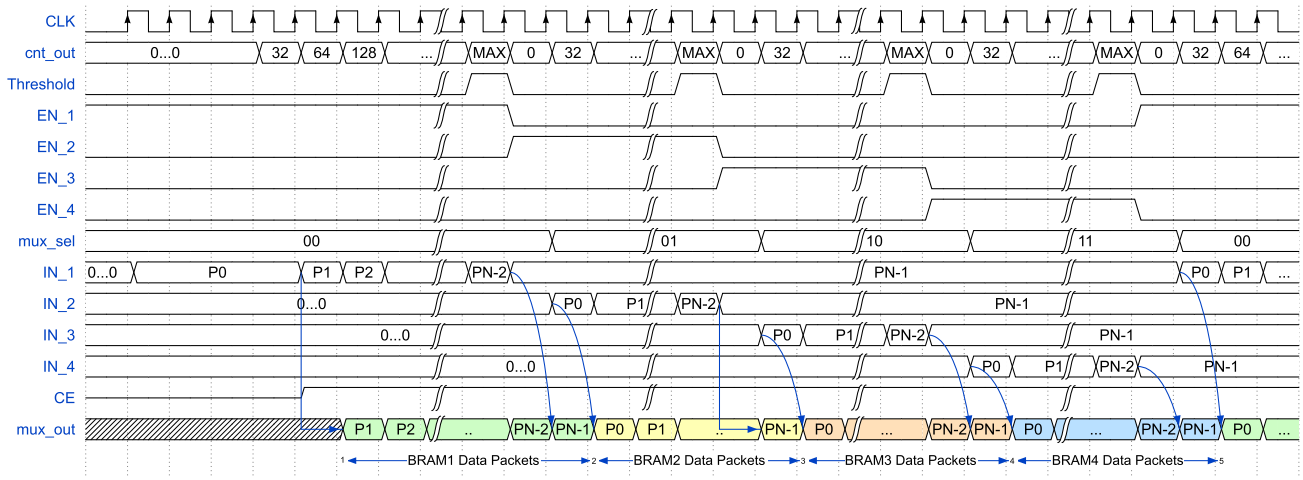


FIGURE 3. Timing diagram of the hardware architecture in the Figure 1.

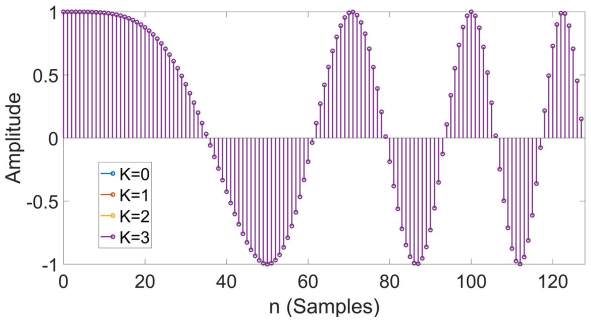


FIGURE 4. Periodic chirp waveform as $s[n + kN] = s[n]$ for $k = 0, 1, 2, 3$.

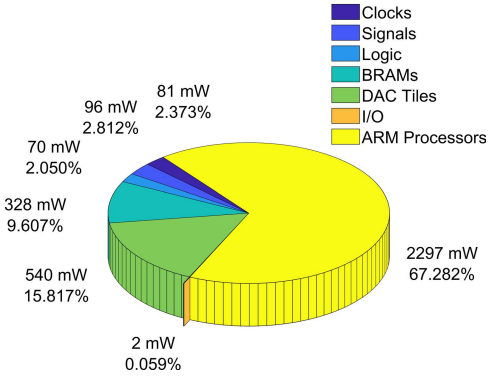


FIGURE 5. Power consumption breakdown of the proposed architecture.

was used with an ultra-wideband amplifier to condition the LO signal for the required drive level of the mixer. The baseband chirp from Channel 1 of the reported synthesizer was passed through a DC block and then low-pass filtered to reduce the harmonics. All ports of the mixer were padded with attenuators to reduce multiple reflections. In addition, the output signal from the mixer RF port was attenuated to reduce third-order products. The upconverted chirp was amplified, filtered with a customized band-pass filter, and passed through a low-pass filter to eliminate extra harmonics in the frequency range of operation of the UWB radar. A 1-km long optical delay line was used for the loopback measurement, and the intermediate-frequency (IF) signal was measured using a high-speed oscilloscope. We used a Keysight M9502A arbitrary waveform generator (AWG) to generate a 500-2200 MHz baseband chirp and upconverted it to compare our chirp generator performance with an off-the-shelf AWG. Figure 7 shows a comparison of the point target response obtained with our chirp generator and the Keysight AWG operating at 60 GSPS along with an ideal point response with a Hanning window. Gaussian noise was added to the ideal response to adjust the noise floor between the measurements and ideal response.

The choice of a window for transforming the time-domain IF signal into the frequency domain involves a trade-off in resolution, near sidelobes, and decay rate of the far-off sidelobes. We used Hanning window because it has low near range sidelobes, 31.5 dB below the main lobe, and 18 dB for octave decay rate for far-off sidelobes as summarized in Table 2 [23], [24]. The high decay rate of the sidelobes is important for identifying multiple reflections in the system and other weak targets. The Blackman-Harris window is also a good choice for analyzing FM-CW radar signals because of its very low first sidelobes and high fall-off rate. However, it has a wide main lobe, which results in degraded resolution. We used a Hanning window to isolate the primary delay line return from multiple reflections. In Figure 7, the asymmetrical nearby sidelobes on both sides of the main lobe and the far-off sidelobes indicate amplitude and phase errors in the chirp and radar system [25].

To compensate for the phase and amplitude errors, we assume that an ideal transmit chirp can be expressed as follows:

$$x(t) = e^{j(\omega_0 t + \pi \alpha t^2)} \tag{9}$$

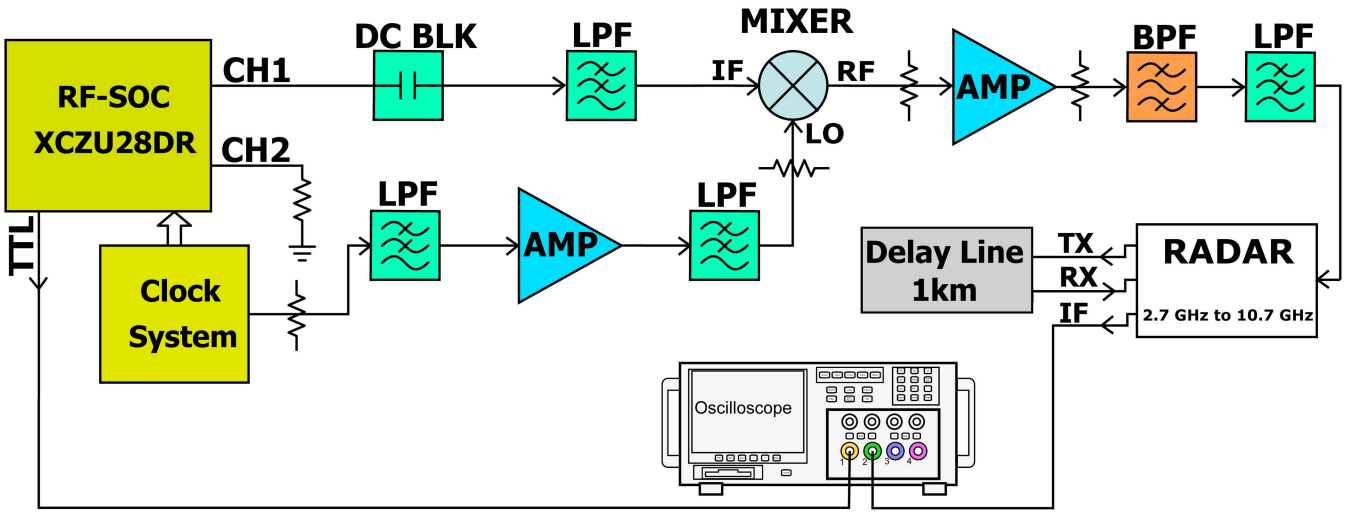


FIGURE 6. RADAR measurement test-bench block diagram.

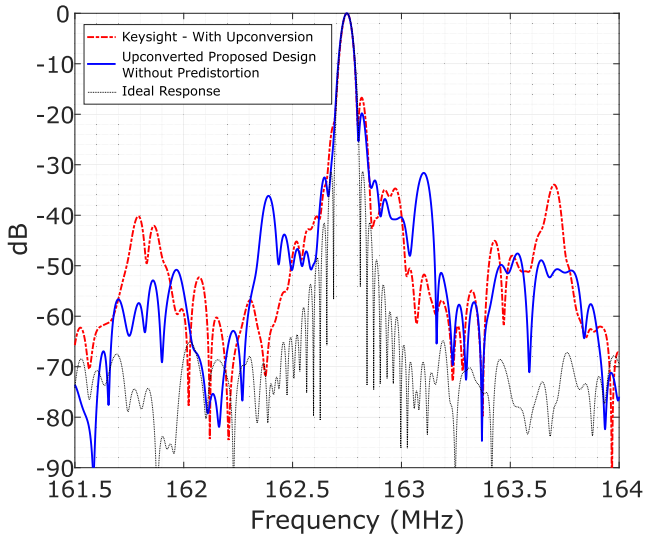


FIGURE 7. Measured IF response of the radar.

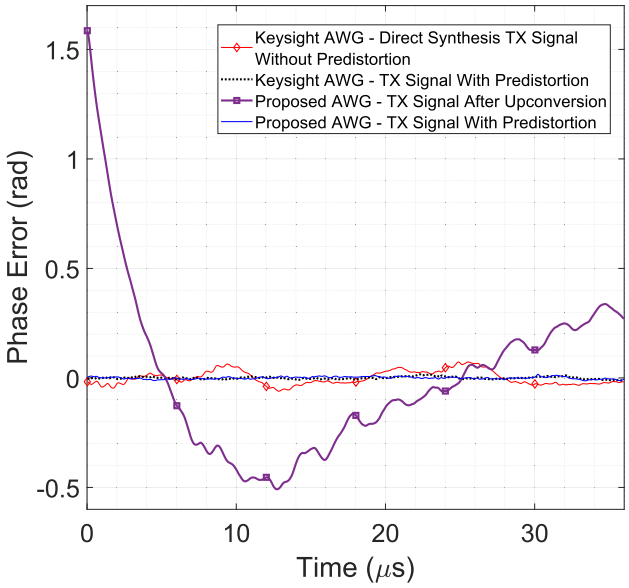


FIGURE 8. Comparison of phase errors in transmit chirp.

Now, consider the transmit chirp, with both amplitude and phase errors, is measured with an oscilloscope as follows:

$$x_d(t) = A_0[1 + ma(t)]e^{j(\omega_0 t + \pi\alpha t^2 + \phi(t))} \tag{10}$$

By multiplying $x_d(t)$ by $x^*(t)$, the amplitude and phase errors can be determined as follows:

$$x_e(t) = x_d(t)e^{-j(\omega_0 t + \pi\alpha t^2)} \tag{11}$$

Which results in:

$$x_e(t) = A_0[1 + ma(t)]e^{j\phi(t)} \tag{12}$$

where $\phi(t)$ is the unwrapped phase of $x_e(t)$ and $[1 + ma(t)]$ is the envelope of the $x_e(t)$. After obtaining the phase and amplitude errors owing to the memory-based architecture of the proposed system, any waveform data can be generated and downloaded into the BRAMs. Thus, we can predistort the transmit chirp such that the final synthetic upconverted chirp is almost free from phase and amplitude errors. In this regard, the upconverted chirp was digitized using a high-speed oscilloscope with a sampling rate of 25 GSPS. The measured phase errors in the transmit chirp over the frequency range of 3.572-5.272 GHz before and after predistortion is shown in Figure 8.

As shown in Figure 8, polynomial and sinusoidal phase errors occur after upconverting the baseband chirp to the higher frequency band. The polynomial error can be attributed to the group delay of the band-pass filter, which has a sharp cut-off. The measured group delay and S-parameters of the fabricated band-pass filter are shown in Figure 9. We had to use a band-pass filter with a sharp cut-off to

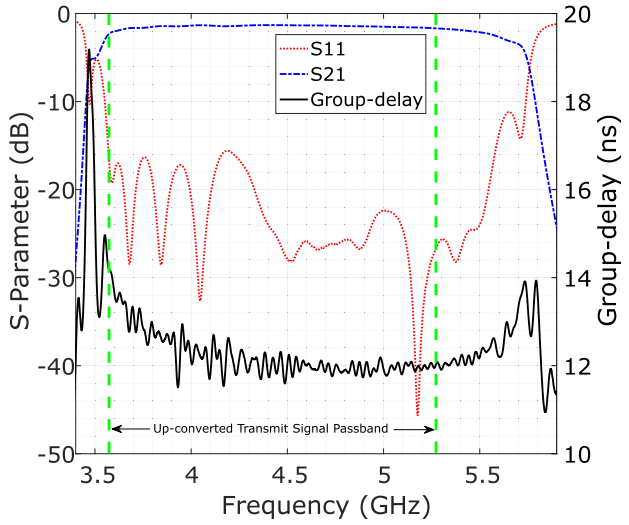


FIGURE 9. Measured S-parameters and group delay of the customized band-pass filter.

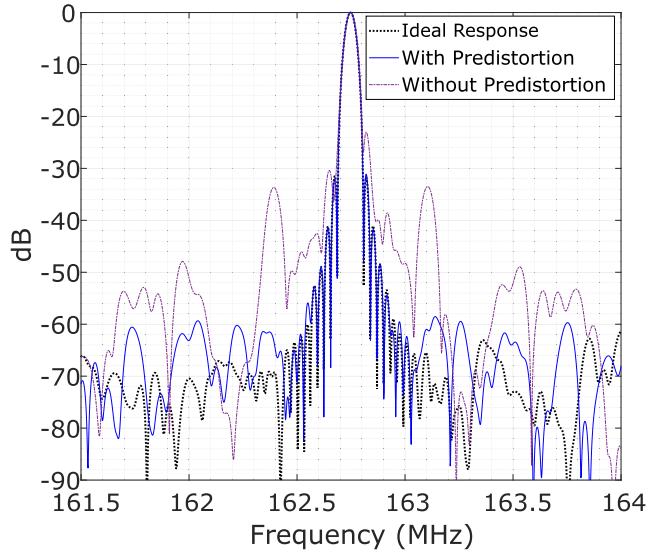


FIGURE 10. IF signal simulation in a 1 km long optical-delay line using the measured synthetic chirp from RF-SoC.

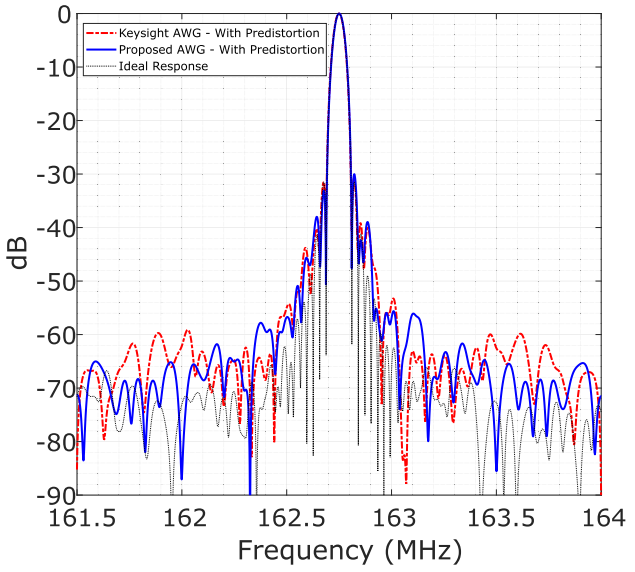


FIGURE 11. Measured IF response of radar after predistortion.

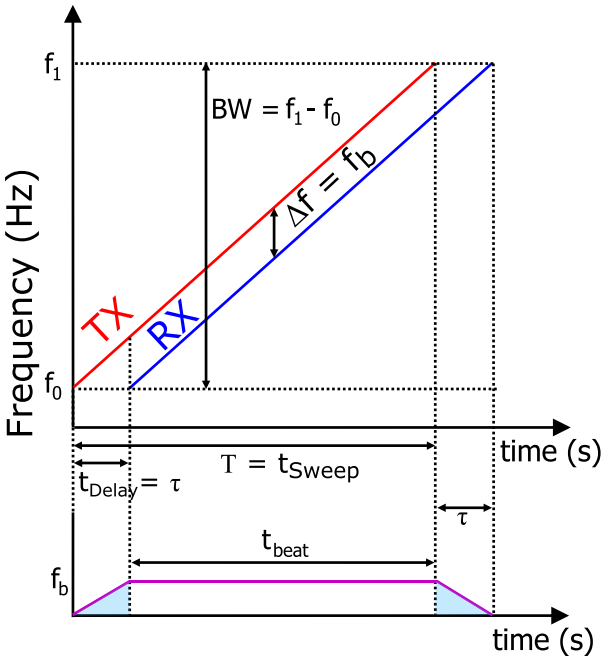


FIGURE 12. The FM-CW concept with beat signal timing.

reduce the LO leakage of the mixer from degrading radar performance. As shown in Figure 9, group delay of the band-pass filter near the lower edge of the pass-band varied from 12-14 ns. We were able to predistort the upconverted transmit chirp to reduce the phase errors to near zero, as shown in Figure 8. We attribute the remaining small phase errors in the transmit chirp to the quantization effect on the downloaded data into memories, DAC nonlinearities, and errors in the measurement instruments and cables. To validate our experiment, a linear chirp with 1.7 GHz bandwidth was directly synthesized from 3.572-5.272 GHz using the Keysight AWG to avoid upconversion process. As shown in Figure 8, a ripple can be observed in the phase error of the chirp that was directly synthesized by the Keysight AWG. This ripple is suppressed using the aforementioned predistortion approach. The phase errors between our work and the Keysight AWG after predistortion show relatively identical results; both are close to zero.

In addition, we developed an ideal FM-CW radar simulator to characterize the measured chirp. Figure 10 shows the simulation results of an ideal FM-CW radar point target response for the digitized chirp with and without predistortion, along with an ideal response. As shown in Figure 10, the simulation results indicate that the phase and amplitude predistortions improve the IF signal performance.

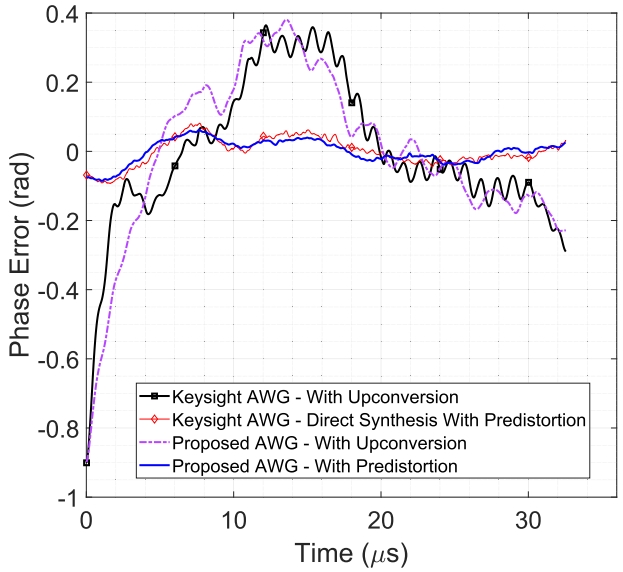


FIGURE 13. Measured phase errors in receiver.

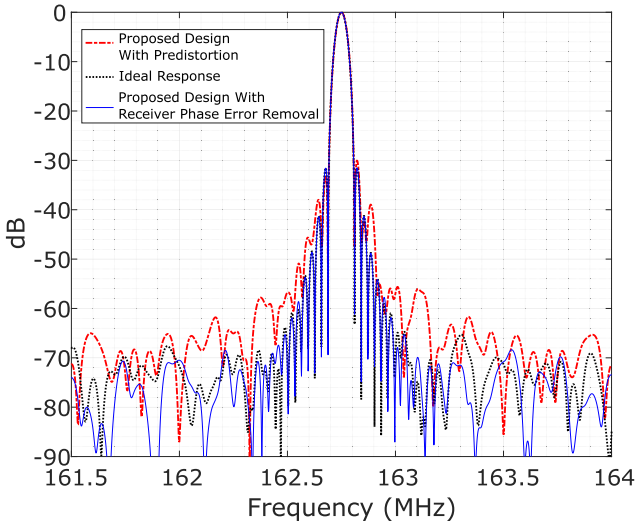
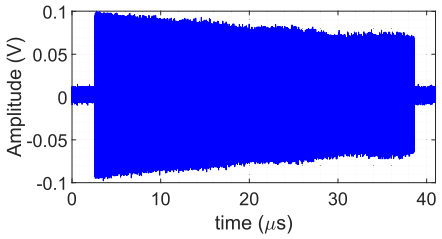
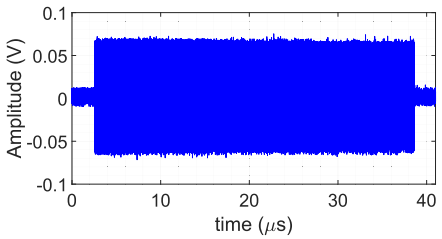


FIGURE 14. Measured IF response with receiver phase errors removal in post-processing.

We also evaluated our corrected upconverted chirp characteristics by measuring the radar IF signal and comparing it with a directly synthesized predistorted chirp over the frequency range of 3.575-5.275 GHz using the Keysight AWG, as shown in Figure 11. As can be observed in the solid curve in Figure 11, the leading and trailing edges of the first sidelobe deviated by approximately 2 dB from the ideal for our chirp, which agrees with the results measured with the Keysight AWG chirp. After correcting phase and amplitude errors in the transmit chirp from our proposed design, the asymmetrical sidelobes in solid curve in Figure 11, are a result of quartic phase errors [25]–[27]. This caused a 2 dB deviation from the ideal response for our predistorted chirp and can be interpreted as the residual phase and amplitude errors introduced by the radar receiver. To further reduce



(a) measured FM-CW chirp signal before applying amplitude corrections



(b) measured FM-CW chirp signal after applying amplitude corrections

FIGURE 15. Suppressing amplitude modulations in transmit chirp with predistortion.

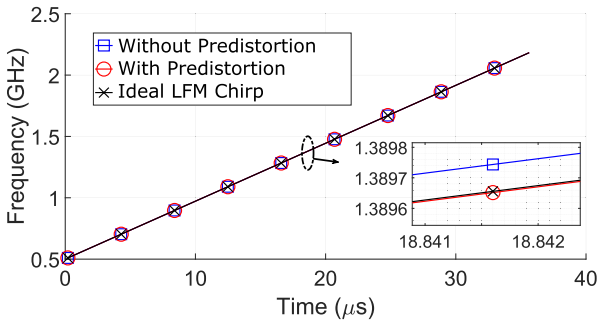


FIGURE 16. Measured baseband chirp frequency versus time.

TABLE 1. Resource utilization report of the proposed design.

Type	Used	Available	Utilization Percentage (%)	Power Consumption (W)
CLB	4345	53160	8.17	0.005
LUT as logic	11045	425280	2.60	0.021
LUT as memory	2819	213600	1.32	0.044
Block Ram Tile	128	1080	11.85	0.328

these errors, we assume that y(t) is an ideal IF signal, which is modelled as follows:

$$y_{ideal}(t) = e^{j\pi(2f_0\tau + 2\alpha\tau t - \alpha\tau^2)} \tag{13}$$

where τ is the amount of delay (t_{Delay}) for the arrival of the received signal, which is equal to $2R/c$ and t is the duration of the beat signal (t_{beat}), as shown in Figure 12. The

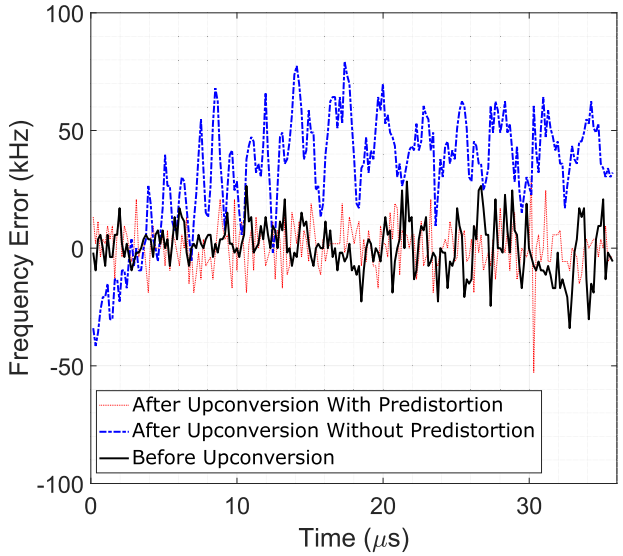


FIGURE 17. Comparison of frequency errors before and after corrections.

TABLE 2. Comparison of different windowing functions.

Window	Peak Sidelobe (dB)	Sidelobe Roll-off (dB/octave)	3-dB BW (BINS)	6-dB BW (BINS)
Rectangle	-13	6	0.89	1.21
%25 Tukey	-14	18	1.01	1.38
Triangle	-27	12	1.28	1.78
Hanning	-32	18	1.44	2
Hamming	-43	6	1.3	1.81
Blackman	-58	18	1.68	2.35
Blackman-Harris	-92	6	1.9	2.72

measured received signal with phase errors in the receiver can be formulated as:

$$y_{received}(t) = e^{j(\pi(2f_0\tau+2\alpha\tau t-\alpha\tau^2)+\phi_{rdl}(t))} \tag{14}$$

where $\phi_{rdl}(t)$ is residual phase error from the receiver and delay line. Using Equations (13) and (14), one can obtain the phase errors in the receiver after multiplying the $y_{received}(t)$ by $y^*_{ideal}(t)$ as follows:

$$e^{j\phi_{rdl}(t)} = y_{received}(t)y^*_{ideal}(t) \tag{15}$$

Figure 13 shows measured phase errors in the receiver. This is verified by obtaining the receiver phase errors, when the Keysight AWG was used to synthesize the input chirp to the radar. It is possible to compensate for the receiver phase errors in post-processing stage. In this regard, after obtaining the phase errors of the receiver using Equation (15), we can eliminate these errors by multiplying the measured received signal by $e^{-j\phi_{rdl}(t)}$. Figure 14 shows the IF signal measurement results from our proposed system, after eliminating the receiver phase errors in post-processing stage. As can be seen in Figure 14, the measured IF signal matches the ideal response after removal of the receiver phase errors. Measurement results show that the proposed chirp synthesizer based on the XCZU28DR can be used in high performance and miniaturized radar applications.

TABLE 3. Performance comparison with some existing works.

Ref.	[8]	[12]	[13]	[31]	This work
Fc (GHz)	38.5	12.15	14.9	19.75	1.350 4.422 *
BW (GHz)	4	0.3	2	8.5	1.7
Percent BW (%)	10.39	2.47	13.42	43.04	125.93 38.44 *
Freq. RMSE (kHz)	4620	167	1210	-	10.49 9.64 *
Linearity Error (%)	0.11	-	-	0.4	0.00062 0.00057 *
Sweep Time (us)	30	3.85	500 to 800	0.06	36
Power Consumption (W)	0.921	0.0338	0.0538	-	3.4
Method	VCO PLL	ADPLL	DDS ADPLL	VCO PLL	RF-SoC

* After upconversion of the baseband chirp with phase and amplitude predistortions.

Figure 15 shows an improvement in removing the amplitude modulations in the measured time-domain FM-CW signal after predistortion. The measured frequency sweep of the transmitted baseband chirp over time is shown in Figure 16. As can be seen, the chirps with and without predistortions are very close to the ideal chirp over the specified bandwidth. The frequency deviation of the synthesized chirps from that of an ideal linear chirp is shown in Figure 17. The RMS frequency error of the predistorted chirp after upconversion process was calculated to be 9.64 kHz. The RMS frequency error before predistorting the upconverted chirp was 40.90 kHz. These measurements indicate that there is around 31.26 kHz of improvement in RMS frequency error after applying the phase and amplitude corrections. Moreover, as shown in Figure 17, a nonlinear trend can be observed in the frequency errors related to the upconverted synthetic chirp without predistortion. After compensating for the phase and amplitude errors with predistortion, the nonlinear trend in the frequency errors was suppressed. The RMS frequency error of the baseband chirp before upconversion was 10.49 kHz as shown by the black curve in Figure 17. The overall chirp linearity could be estimated as the ratio of the RMS frequency error to the full-span chirp bandwidth [28]. With the calculated RMS frequency error of 9.64 kHz in the upconverted chirp with predistortion, a linearity error of 0.00057% is obtained over 1.7 GHz of bandwidth within 36 μs sweep time. Table 3 provides a performance comparison with existing studies in the literature.

As mentioned earlier, one of the applications of chirp radar is in remote sensing of snow and soil moisture. Kim *et al.* reported that to obtain a good estimate of the snow water equivalent (SWE), the radar resolution must be better than 10 cm [29]. This requires a radar with a bandwidth greater than 1.5 GHz, accounting for the weighting of the received signal to reduce the sidelobes. This can be accomplished with our 1.7 GHz wide-band synthetic chirp with a sweep rate of 36 μs from 0.5-2.200 GHz or from 3.572-5.272 GHz with upconversion process. Wu et al. discussed the trade-off between chirp sweep rate, high-resolution velocity detection, and protection of the beat frequency from flicker noise [30].

V. CONCLUSION

A digital chirp generator was designed and implemented on XCZU28DR RF-SoC. Moreover, a memory-stitching concept was proposed to overcome the timing errors in high-speed digital designs. The reported chirp synthesizer can be used to develop UWB FM-CW, stretch and pulse compression radars. Furthermore, a 1.7 GHz LFM chirp signal was synthesized using the proposed architecture, which sweeps the overall bandwidth within 36 μs. The simulation and measurement results show that by predistorting the phase and amplitude errors, the reported system can synthesize a high-precision chirp with negligible deviation from an ideal LFM chirp. Radar loop-back measurements indicate -30 dB sidelobes in the IF signal impulse response using Hanning weighting and show a response comparable to that of a commercially available AWG operating at 60 GSPS. Future work will include stitching the output chirps from each separate channel to achieve a significantly larger bandwidth chirp. In addition, this system can be incorporated into an UWB radar system to collect soil moisture and snow depth data for further investigation and analysis.

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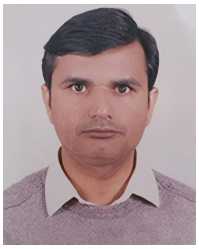

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