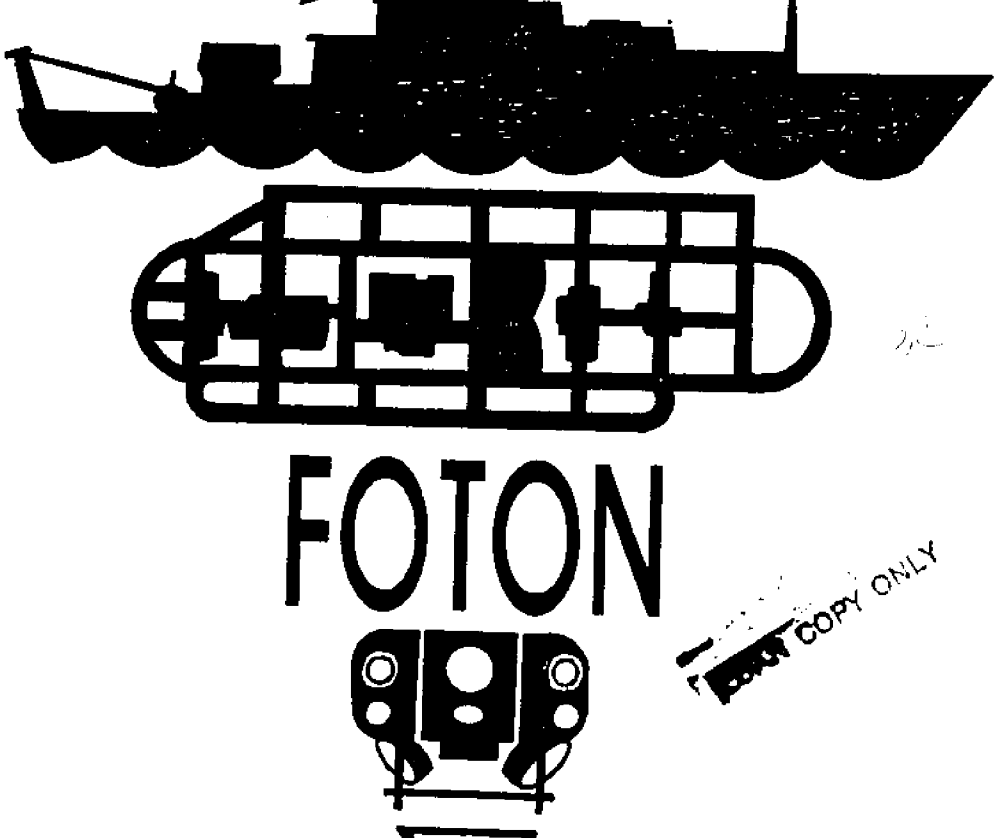

FOTON

UNIVERSITY OF NEW HAMPSHIRE

College of Engineering and Physical Sciences

Sea Grant Ocean Projects 1986-1987

FOTON

Fiber Optic Telemetry Operations Network

Ocean Projects - TECH 697

Final Project Report

Spring 1987

UNIVERSITY OF NEW HAMPSHIRE

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INTRODUCTION

Project FOTON (Fiber Optic Telemetry Operations Network) involves the design and development of a fiber optic communication link between two unmanned deep diving submersible vehicles of the Deep Submergence Lab (DSL) at Woods Hole Oceanographic Institution in Woods Hole, Massachusetts. The link is to be used on the ARGO/JASON system shown in Figure 1 which is designed for deep ocean (20,000 ft.) surveying and scientific research.

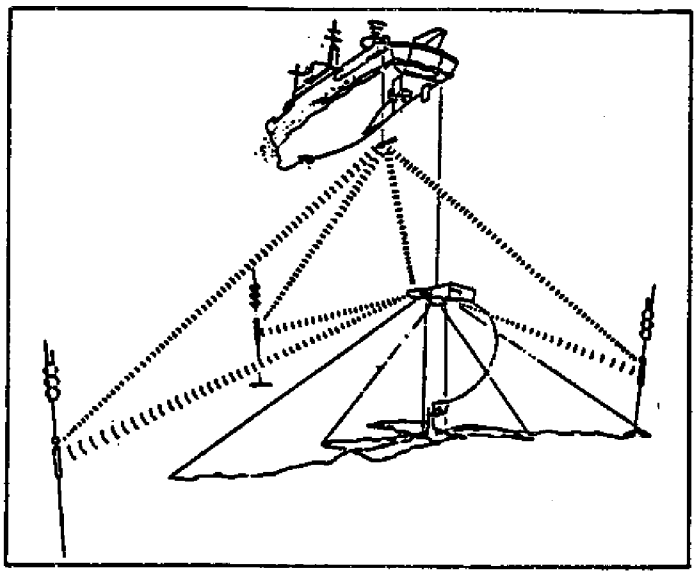


Figure 1: The ARGO/JASON System

The ARGO is an unmanned, sledlike submersible employing both acoustic and optical imaging systems as well as a storage area for JASON, it's remotely operated vehicle (ROV). JASON is a small self-propelled vehicle designed to perform close-up inspection, precision sampling, and manipulative work. It carries two color video cameras and dual robot arms. Project FOTON's goal is to develop a system capable of transmitting the two video signals and the control data from JASON to ARGO.

The large amount of data associated with two video signals dictates the need for an optical fiber to be used as the transmission medium rather than the more conventional coaxial cable. The optical fiber has the large bandwidth capabilities necessary to transmit this amount of data over a significant distance while the coaxial cable does not. The advantages of using an optical fiber are discussed in more detail in a later section of this report. The system requires that these two video signals, each with a 4.2 MHz bandwidth, be transmitted simultaneously with the control or telemetry information which has a comparatively small bandwidth of a few kilohertz. This must be done in a way such that the three signals don't interfere with each other during transmission and can then be easily separated on the recieving end. To accomplish this, two of the three signals must be mixed up away from their baseband frequencies. There are many ways of implementing this. The video signals could be mixed up to frequencies such as 10 MHz and 25MHz while the telemetry is kept in baseband as is shown in the frequency spectrum graph of Figure 2a.

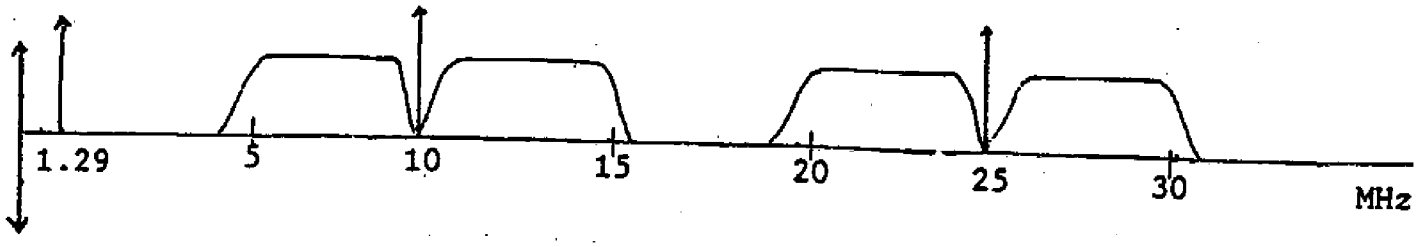


Figure 2a: Input Signal Frequency Spectrum (Scheme 1)

A variation of this scheme is to mix both of the video signals up to 15 MHz but have one in phase and one in quadrature (i.e. they are 90 degrees out of phase with each other), thus not interfering with each other.

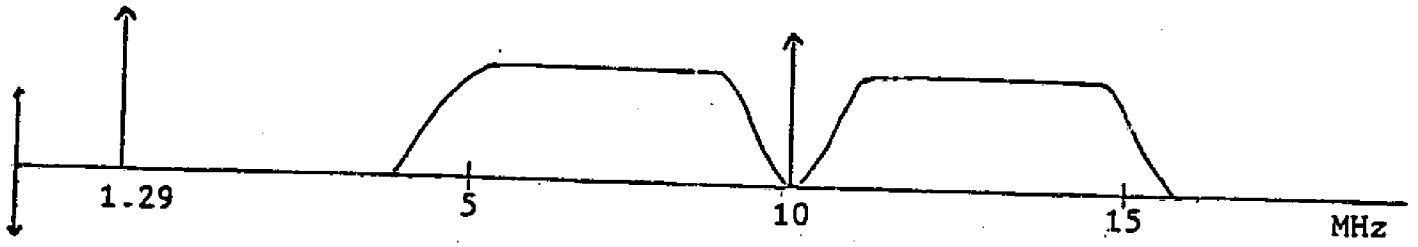


Figure 2b: Input Signal Frequency Spectrum (Scheme 2)

This second scheme, pictured in Figure 2b, uses a total of 20MHz baseband bandwidth as compared to 30MHz for the first scheme. It is important to note, however, that the design and implementation of a mixing and filtering scheme for the three signals is not part of project FOTON's responsibilities. FOTON has recommended the latter of the two schemes mentioned and has designed a system with enough bandwidth capability to implement it.

Aside from the bandwidth requirement, the communication link has a few other specifications to meet. One specification was to use AT&T's ODL 200 Lightwave Data Link, containing the electrical-to-optical (E/O) and optical-to-electrical (O/E) converters, and these imposed several constraints of their own. Thus the circuits we designed had to meet the input and output specifications associated with the lightwave kit (refer to Appendix A). For example, the input to the E/O converter had to be a bilevel signal (varying between two specific voltage levels) whose frequency is within the range $40MHz < f < 220MHz$. Two methods of converting the three input signals into a compatible waveform were investigated. It was decided that models for each method would be developed, the pros and cons of each examined, and the better of the two would then be developed in the final design.

One method took a digital approach to the problem. The two video signals would be digitized using A/D converters and then time multiplexed together with the control data, which can be retrieved in digital form from the CPU in the current JASON system, into frames of information which would then be sent serially over the fiber. Each frame would contain equal amounts of video data bits and a much smaller amount of telemetry bits due to the latter's much slower data rate. One problem we encountered immediately with this scheme involves the regeneration of the system clock at the reciever end which would be necessary to reframe the data coming over the fiber and to recover it. A satisfactory method for clock regeneration in the FOTON system could not be found. In addition, the data rate for this digital system was conservatively estimated at 240 Megabits/sec which exceeds the ODL 200 lightwave kits maximum data rate capability of 220 Megabits/sec.

The second method considered utilizes frequency modulation (FM). The composite input signal would be modulated into a bilevel signal of constant amplitude and varying frequency and could be manipulated so as to satisfy the requirements of the E/O and O/E converters. The modulated signal would then be demodulated at the reciever using some sort of FM detector. The major obstacle to this method was finding devices which could generate and detect FM signals at high enough frequencies.

It was decided that for this project the FM method would have a better chance of success. A more in depth discussion of FM follows in the main report.

ARGO/JASON PRESENT SYSTEM

Description of Operation

Currently, ARGO/JASON utilizes a telemetry I/O system designed by Colmek Systems Engineering which is shown in Figure 3. This system utilizes Frequency Shift Keying (FSK) to modulate the telemetry information for transmission over the highly attenuative coaxial cable. FSK is a way of changing the 9600 baud digital information from the surface and subsurface CPU's to analog signals whereby each distinct digital state ("1" or "0") generates a discrete transmit frequency. These frequencies are received at the other end of the link and decoded back to discrete information states which are then processed by the CPU. This system utilizes two FSK channels, a downlink at 1.52 MHz for vehicle control, and an uplink at 1.29 MHz for vehicle information. The single video channel in this system is frequency modulated using a voltage controlled oscillator (VCO) with a carrier frequency of 32MHz and is demodulated using a quadrature detector.

The proposed FOTON system would utilize the FSK and simply add the two video signals in above it. The mixing scheme suggested in the last section and shown in Figure 2b could be implemented with a system like that shown in Figures 4 & 5. The summing op-amp in the transmitter circuit must have unity gain over the entire baseband bandwidth, and filtering must be done at the reciever end to separate the signals.

Present System Limitations and FOTON'S Improvements

The limitations of the present system lay mostly in the use of a coaxial cable as a transmission medium. The metal conductors in the cable have maximum data rate capability which the system is near approaching. Therefore, imposing additional information to this system requires a redesigning of the cable to accommodate the higher data rates. Also, the use of this type of cable is very restrictive to the tether management system which controls the reeling in and out of the cable as JASON swims around. The twisting and tensile forces caused by the weight and size of a coaxial cable make the tether extremely difficult to manage as its length increases.

Project FOTON utilizes an optical fiber for data transmission which is capable of carrying substantially higher data rates with less loss than a coaxial or twisted-pair type cable. Figure 6 shows the attenuation vs. frequency for three types of transmission lines.

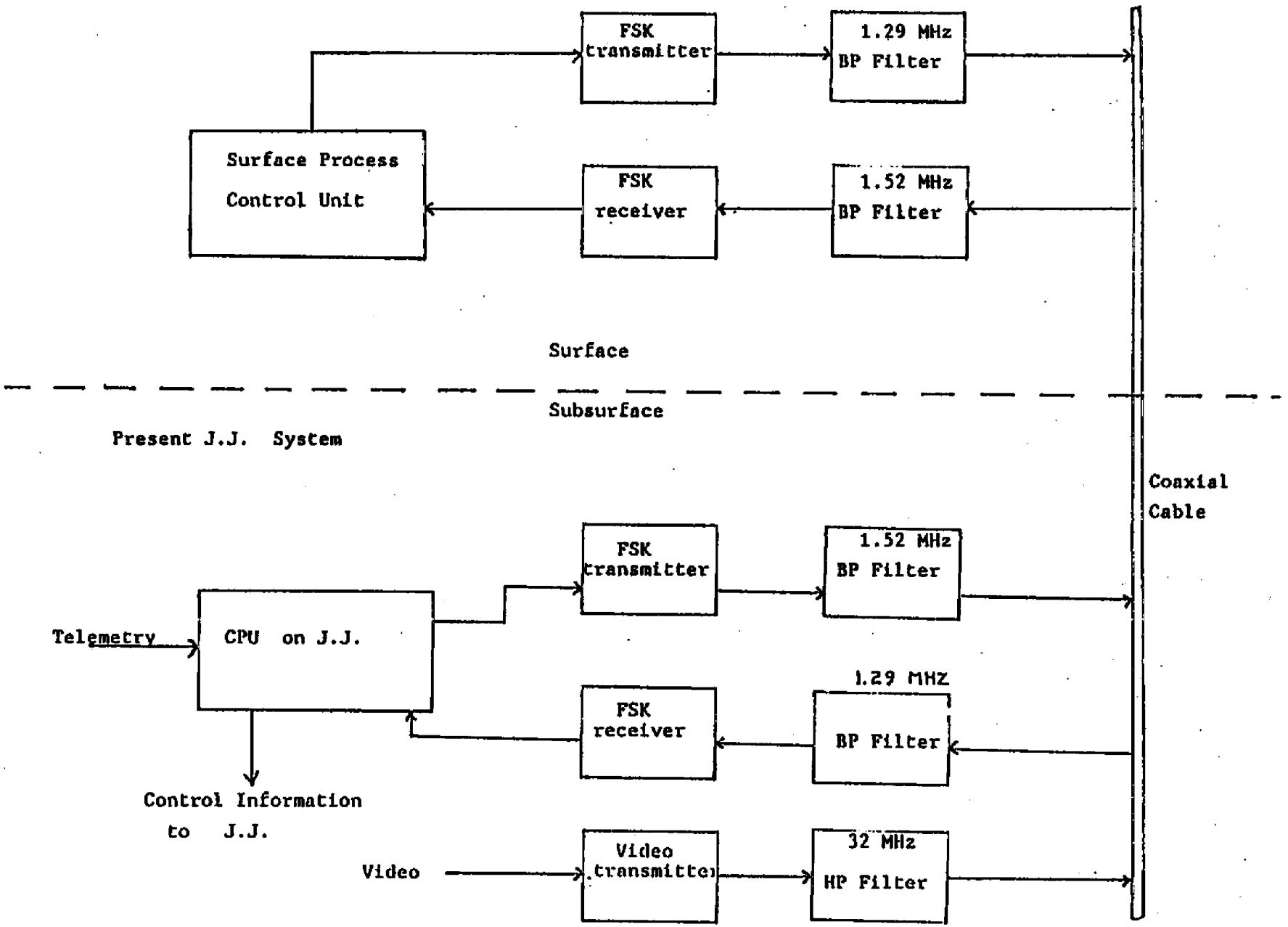


Figure 3 - Current ARGO/JASON I/O system.

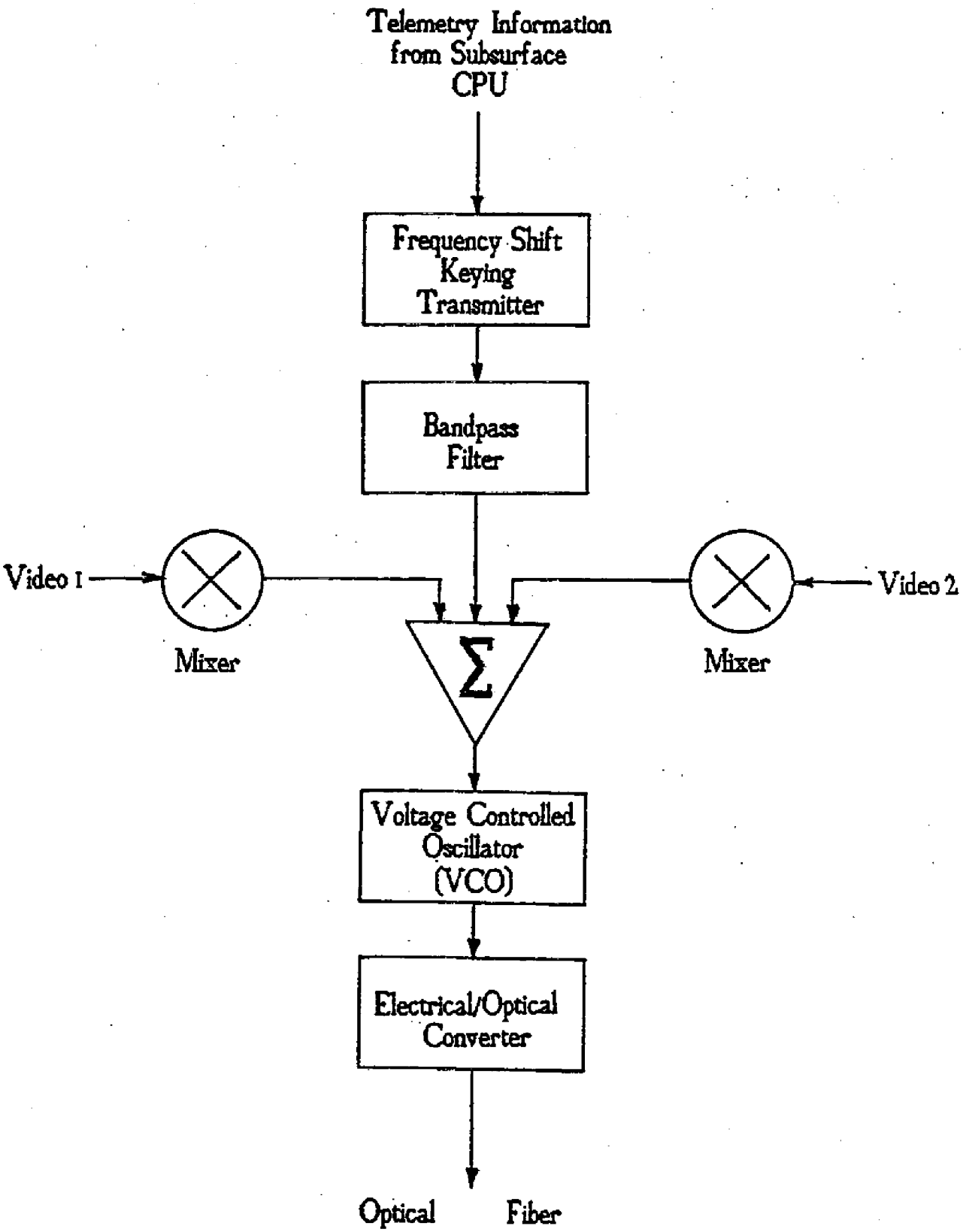


Figure 4 - Possible JASON transmitter block diagram.

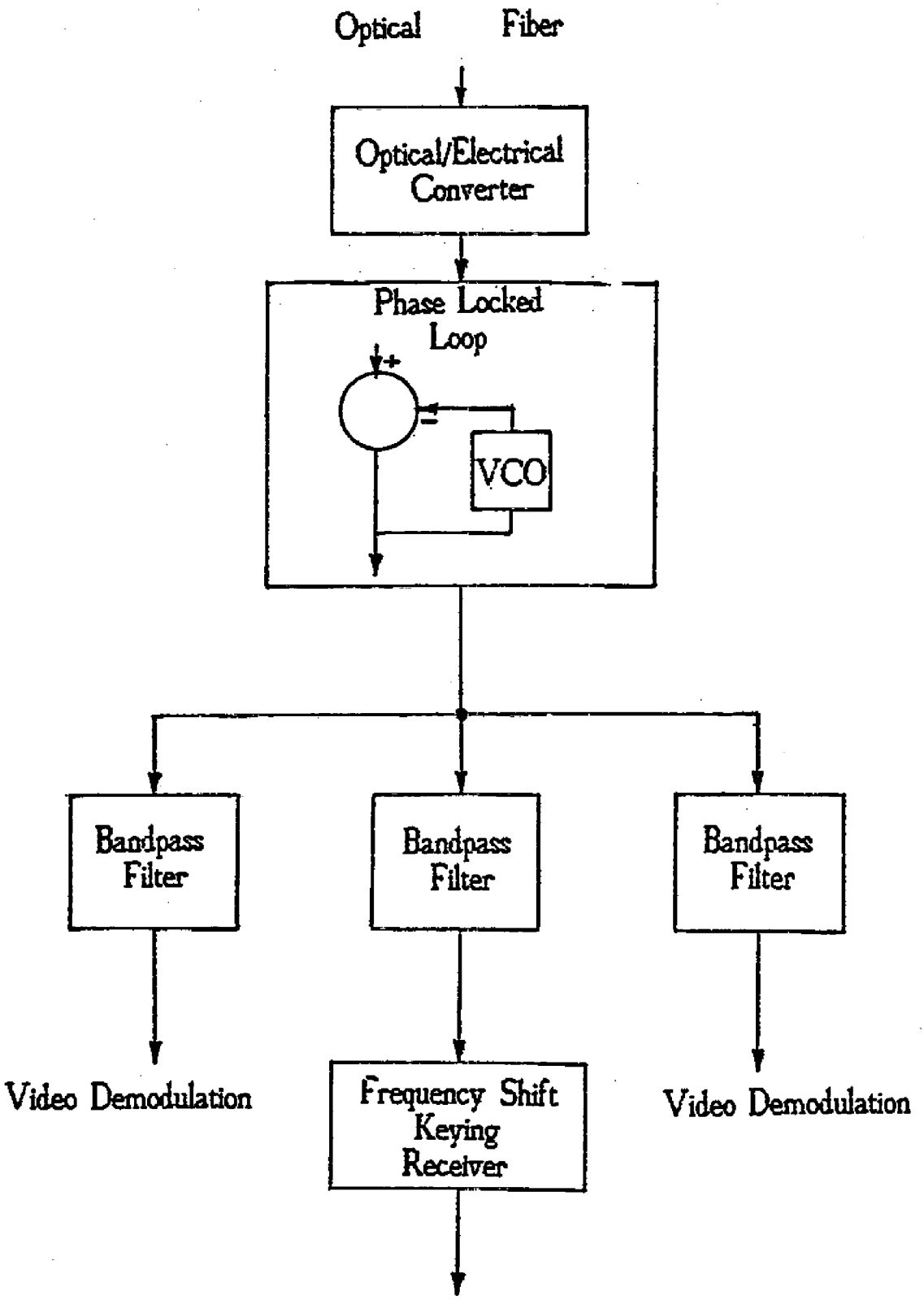


Figure 5 - Possible ARGO receiver block diagram.

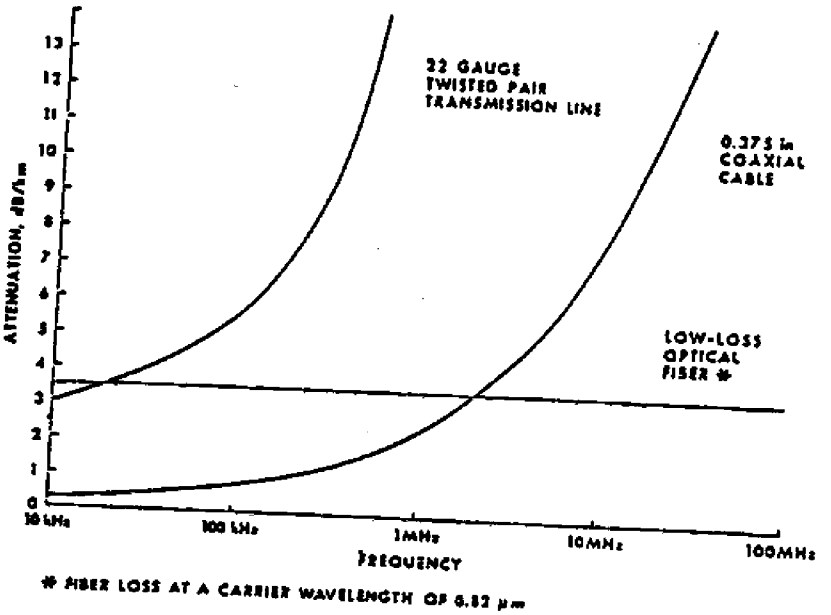


Figure 6: Attenuation vs. Frequency for 3 Types of Transmission Lines.

While attenuation increases dramatically at higher data rates for metallic transmission lines, the optical waveguides loss remains fairly constant. This high bandwidth capability is conducive to DSL's plans to add an additional color video camera on JASON for stereo viewing which wasn't previously possible with a coaxial transmission line.

Because it is nonconductive, nonradiative, and noninductive the optical fiber is less susceptible to problems such as radiative interference and ground loops which may cause problems in systems utilizing metallic conductor type transmission lines. The fiber is also much smaller in diameter and lighter than the coaxial cable, thus putting less stress on the launch and retrieval system and making the tether easier to manage overall. Probably the most attractive aspect of introducing an optical fiber to the system is the potential for future growth. Not only will stereo vision be possible, but the optics provide capacity for additional high data rate instuments for more optimal control or measurement as well.

FM THEORY

Project FOTON selected frequency modulation (FM) as a means to transmit information over the optical fiber. "In contrast to linear modulation (such as amplitude modulation), FM is a type of exponential modulation which is a non-linear process; therefore the modulated spectrum is not related to the message spectrum in a simple fashion. Moreover, it turns out that the transmission bandwidth is usually much greater than twice the message bandwidth. Compensating for this bandwidth liablility is the fact that FM can provide increased signal-to-noise ratios (SNR's) without increased transmitted power. FM thus allows one to trade bandwidth for power in the design of a communication system."[1] Utilization of an optical fiber provides the necessary bandwidth to use FM and benefit from improved SNR's.

In FM, the instantaneous frequency F(t) varies above and below the carrier frequency Fc by an amount $\pm F_\Delta X(t)$. Where F_Δ is known as the frequency deviation and X(t) is the instantaneous value of the modulating (input) signal. If Am is the maximum amplitude of the modulating signal, then the furthest F(t) can deviate from Fc is

$$\pm F_\Delta X(t)max = \pm F_\Delta Am = \pm \Delta F \qquad \text{eqn 1}$$

In general, the larger F is compared to the frequency one is trying to modulate (Fm), the better the SNR. This ratio is known as the FM modulation index β.

$$\beta = \frac{F_\Delta Am}{Fm} = \frac{\Delta F}{Fm} \qquad \text{eqn 2}$$

The transmission bandwidth (BW) of the modulated signal being transmitted over the fiber can be estimated using Carson's Rule to be:

$$BW = 2(\Delta F + Fm) \qquad \text{eqn 3}$$

This estimate includes approximately 90% of the transmitted power spectrum. It can be shown that the SNR for an FM system is:

$$SNR_{FM} = 1.5\ B^2 \gamma \qquad \text{eqn 4}$$

where γ = SNR max for baseband, single sideband , and double sideband systems. FM, therefore, has an inherent improvement in SNR over these other types of modulation by a factor of $1.5B^2$, known as the FM improvement factor.

1 - Carlson, A. Bruce, 1975: "Communication Systems", second ed. McGraw-Hill, New York, NY.

GENERATION AND DETECTION OF FM SIGNALS

FM Generation: The Voltage Controlled Oscillator

Direct generation of FM requires a device whose oscillation frequency has a linear dependence on its applied voltage. Project FOTON uses a voltage controlled oscillator (VCO) for this purpose. Available commercially, VCO's will deviate by an amount ± F above and below a center frequency, Fc, which the user specifies with various biasing components. The amount the VCO deviates about Fc depends on the gain or frequency deviation F of the oscillator and the amplitude of the input, Am (Refer to eqn 1). It is important to note that the relationship between input voltage and output frequency must be linear over the entire range of F and this puts a limit on how large F can be for a given center frequency Fc. This maximum value of F is usually expressed as a percentage of Fc and ranges from 10-20% depending on the model and make of the VCO.

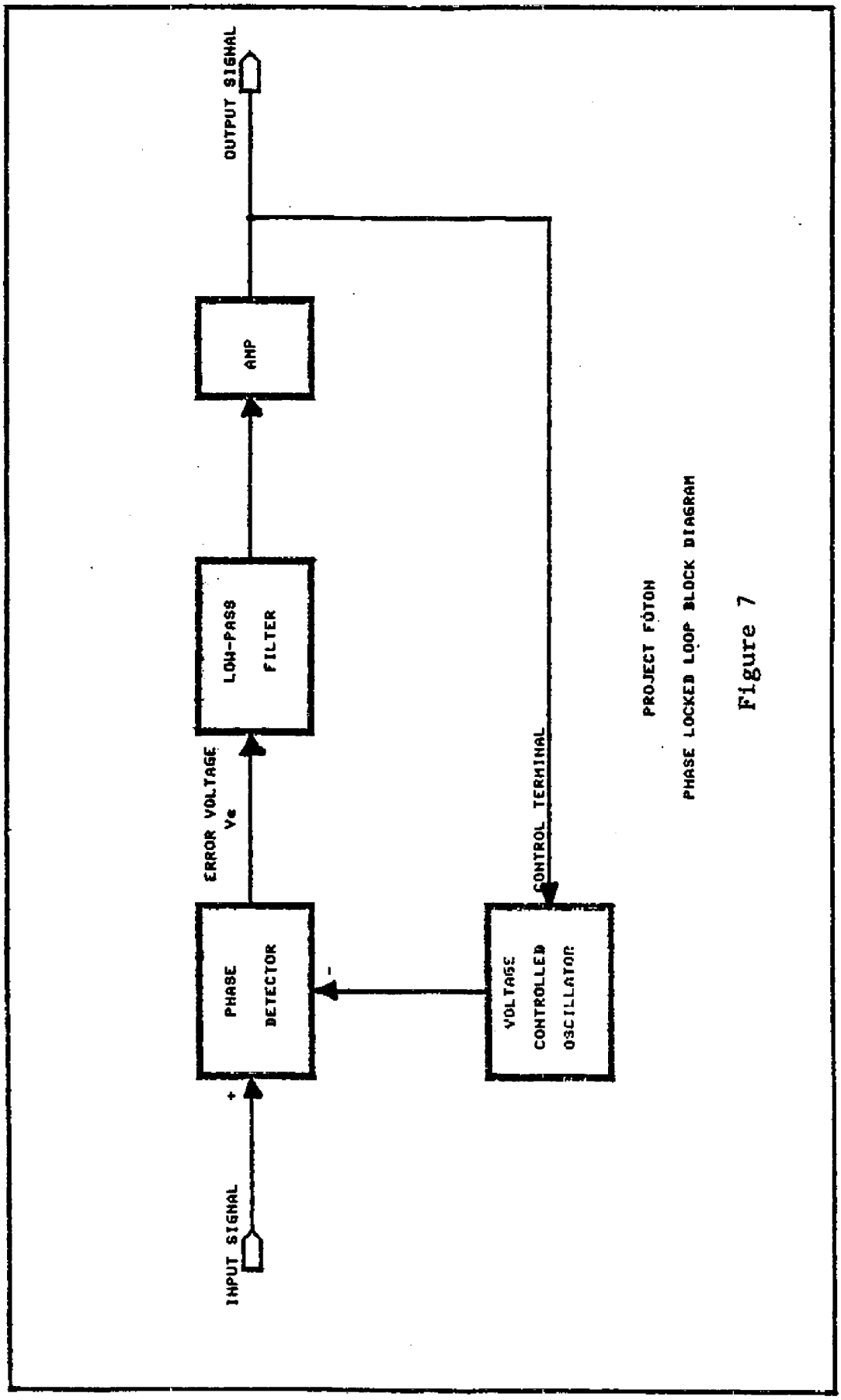
In order to achieve high SNR, a high β and therefore a high F are required for a given Fm (refer to eqns 2 thru 4). This in turn means Fc must be increased since ΔF is limited to a certain percentage of Fc which leads to the general conclusion that the faster you run the VCO, the better the SNR. Of course the tradeoff associated with FM still exists here. As the speed of the VCO is increased to improve the SNR, more bandwith is required to handle the modulated signal.

FM Detection: The Phase Locked Loop

One way to detect FM signals is by using a Phase Locked Loop (PLL). The PLL is a feedback system composed of a phase comparator, a low pass filter, an error amplifier in the forward signal path and a VCO (described above) in the feedback path. A block diagram of a basic PLL system is shown in Figure 7. The basic operation of a PLL can be described as follows:

With no input voltage applied to the circuit the VCO operates at its center or free-running frequency Fc. The phase comparator compares the phase and frequency of the input with the VCO output and generates an error signal Ve which is proportional to the difference between the two. This error signal is then filtered and amplified and then applied to the control terminal of the VCO. The nature of the negative feedback loop is to drive the error signal to zero and thus force the VCO to oscillate at the same frequency as the input to the loop. When this happens the loop is said to be "in lock" and the voltage holding the VCO in lock with the input to the loop appears at the output of the loop. Thus the PLL exactly reverses the function of a VCO alone and achieves demodulation of the FM signal.

Once the loop is in lock, the self-correcting nature of the system allows it to track changes in the input frequency over fairly wide ranges and remain in lock. The range of input frequencies over which the PLL can mantain lock is known as the "Lock Range", and the range of frequencies over which the PLL can acquire lock is known as the "Capture Range". The capture range is always smaller than the lock range and both are centered about Fc.



PROJECT FÖTON

PHASE LOCKED LOOP BLOCK DIAGRAM

Figure 7

LOW FREQUENCY MODEL

It was decided by the FOTON team that a low frequency model of the proposed system should be designed, built, and tested. This gave the team members valuable experience in dealing with the problems which arose when using VCO's and PLL's, and also proved the validity of the theory upon which the system design was based.

The model consisted of a VCO connected by a coaxial cable to a PLL as is shown in the block diagram of Figure 8. Due to their availability, two EXAR XR-215 monolithic PLL chips (see Appendix B for specifications) were used in implementation of the modulator and demodulator circuits. Examination of the pinout diagram for the XR-215 (Figure 9) indicates that the VCO in the feedback path of the loop is easily accessible.

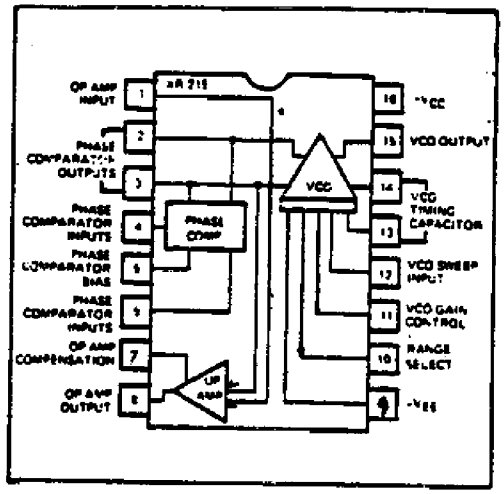


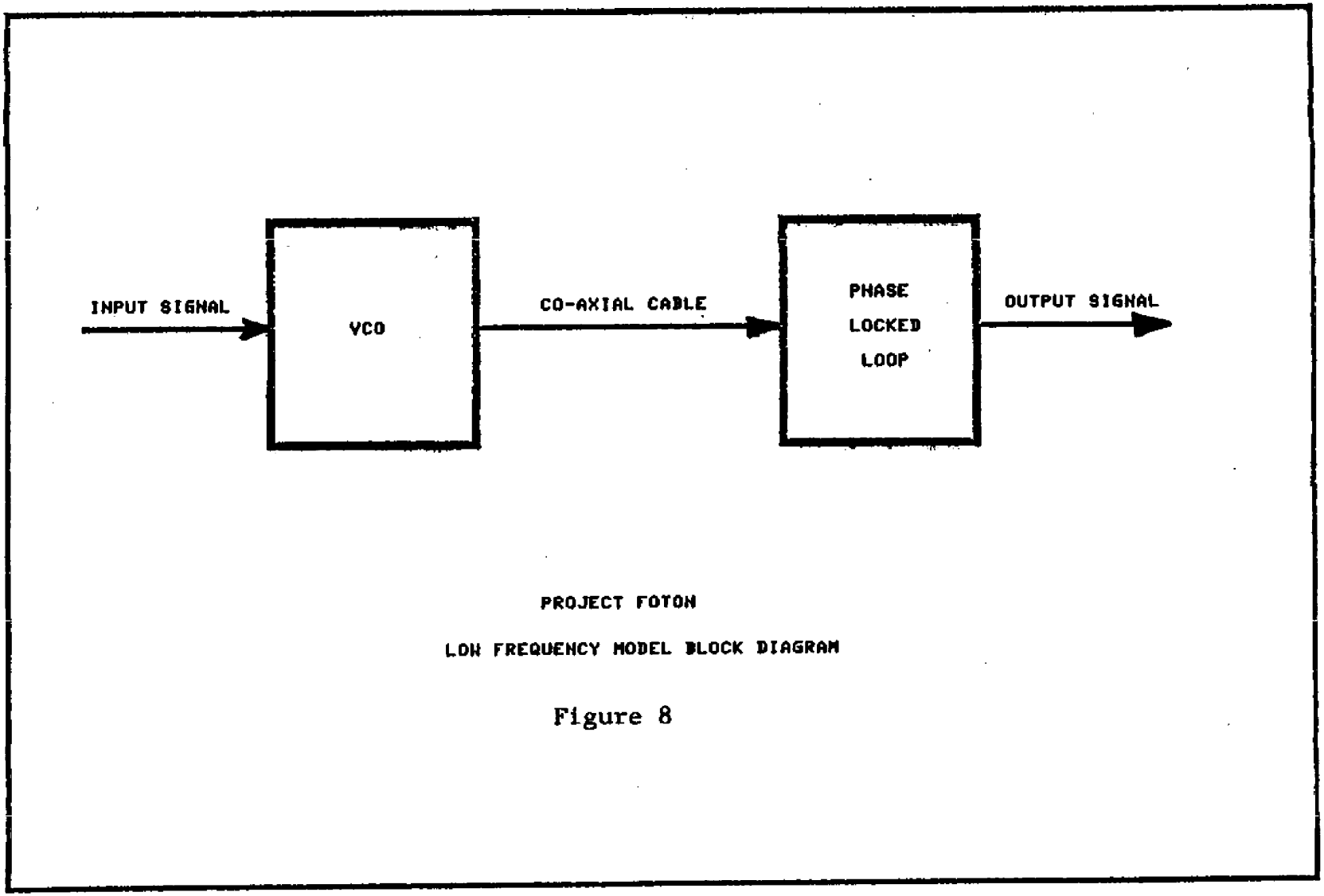
Figure 9: XR-215 Pinout Diagram

By forcing the modulating (input) waveform onto the control pins of the VCO (pins 11 and 12) the output of the VCO is FM and thus we can implement the modulator of Figure 10. The free-running frequency of the VCO can be approximated as

$$Fc = \frac{0.0002}{Co}\left[1 + \frac{600}{Rx}\right]$$

where Co = 160 pF and Rx = 750 Ohms were chosen as biasing values so as to modulate the signal at a center frequency Fc = 1MHz. The demodulator circuit (Figure 11) was required to run at the same frequency and therefore the same values for Co and Rx were used.

The design was wire-wrapped and tested by applying sine waves and audio signals to the input. It was determined that the system could successfully modulate and demodulate a signal with a maximum bandwidth of approximately 100KHz, nowhere near enough for video transmission but enough to handle audio. As expected the knowledge and experienced gained by developing the low frequency model proved invaluable when it came to testing and debugging the high frequency system.



PROJECT FOTON

LOW FREQUENCY MODEL BLOCK DIAGRAM

Figure 8

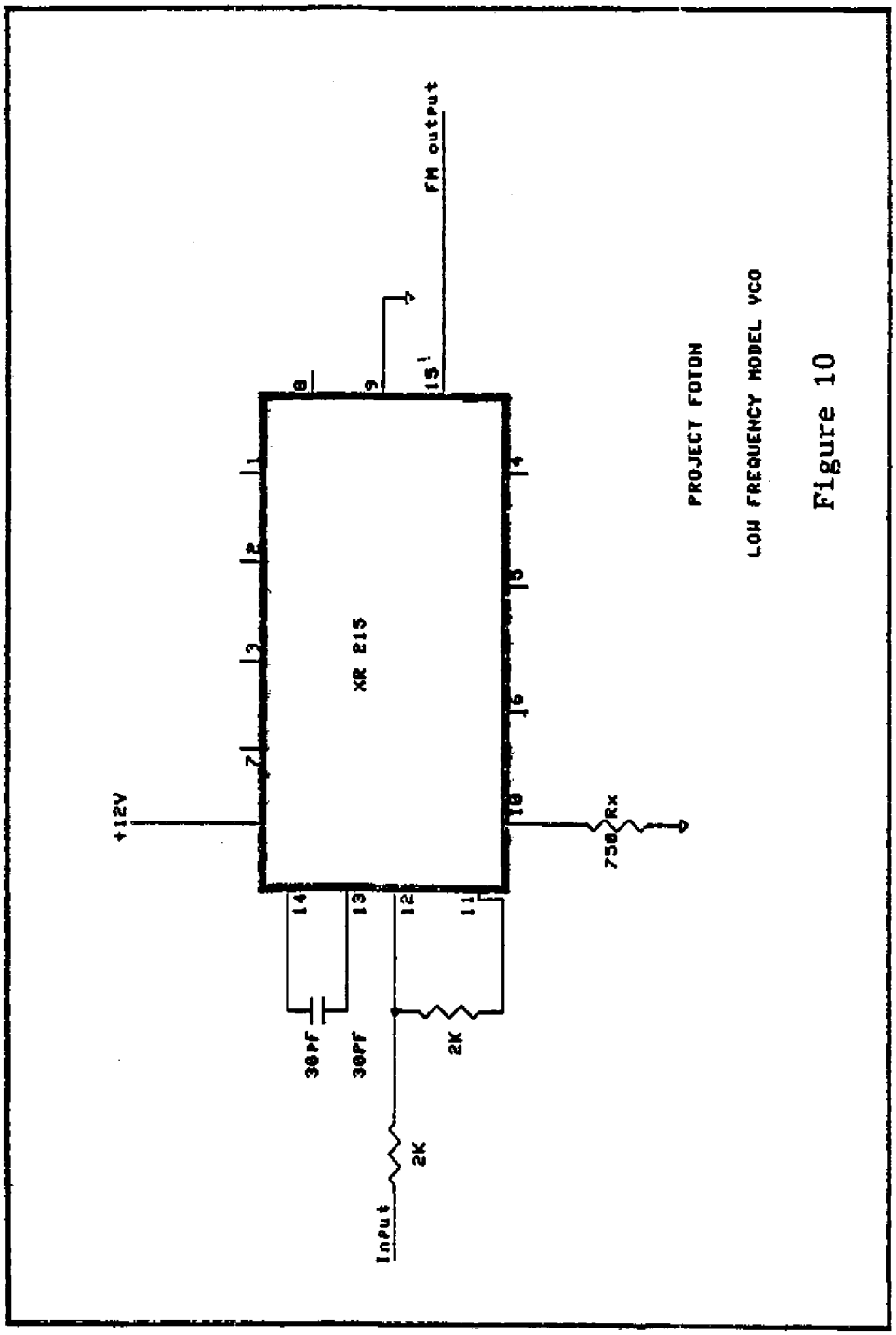

PROJECT FOTON
LOW FREQUENCY MODEL VCO
XR 215
+12V
FM output
Input
2K
30PF
30PF
2K
750
Rx

Figure 10

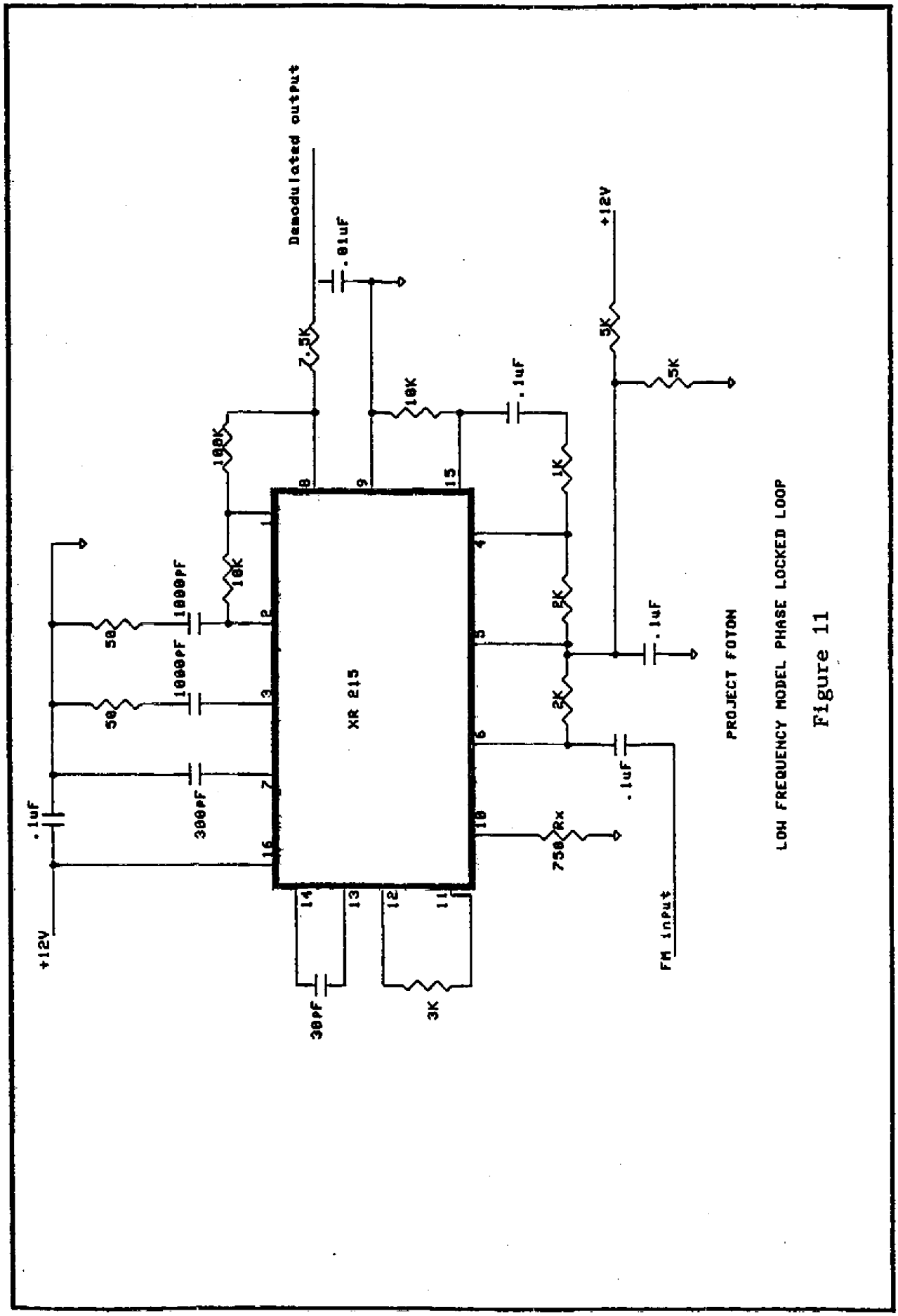

Demodulated output
.01uF
7.5K
10K
.1uF
+12V
5K
5K
100K
1K
10K
1000pF
50
1000pF
50
2K
.1uF
XR 215
2K
.1uF
.1uF
300pF
Rx
750
+12V
FM input
30pF
3K
PROJECT FOTON
LOW FREQUENCY MODEL PHASE LOCKED LOOP

Figure 11

THE FOTON SYSTEM

A high level block diagram of the FOTON system appears in Figure 12. Each block shown will be discussed separately in this part of the report. A 150MHz PLL manufactured by Signetics Corp. (part# NE-568) was used in the system design to achieve high frequency FM generation and detection. Only the VCO section of the chip was used for FM generation while the entire chip was used for FM detection. A diagram of the internal chip functions and pinouts for the NE-568 appears in Figure 13 and the chip specifications are found in Appendix C.

THE TRANSMITTER

The NE-568 as an FM Generator

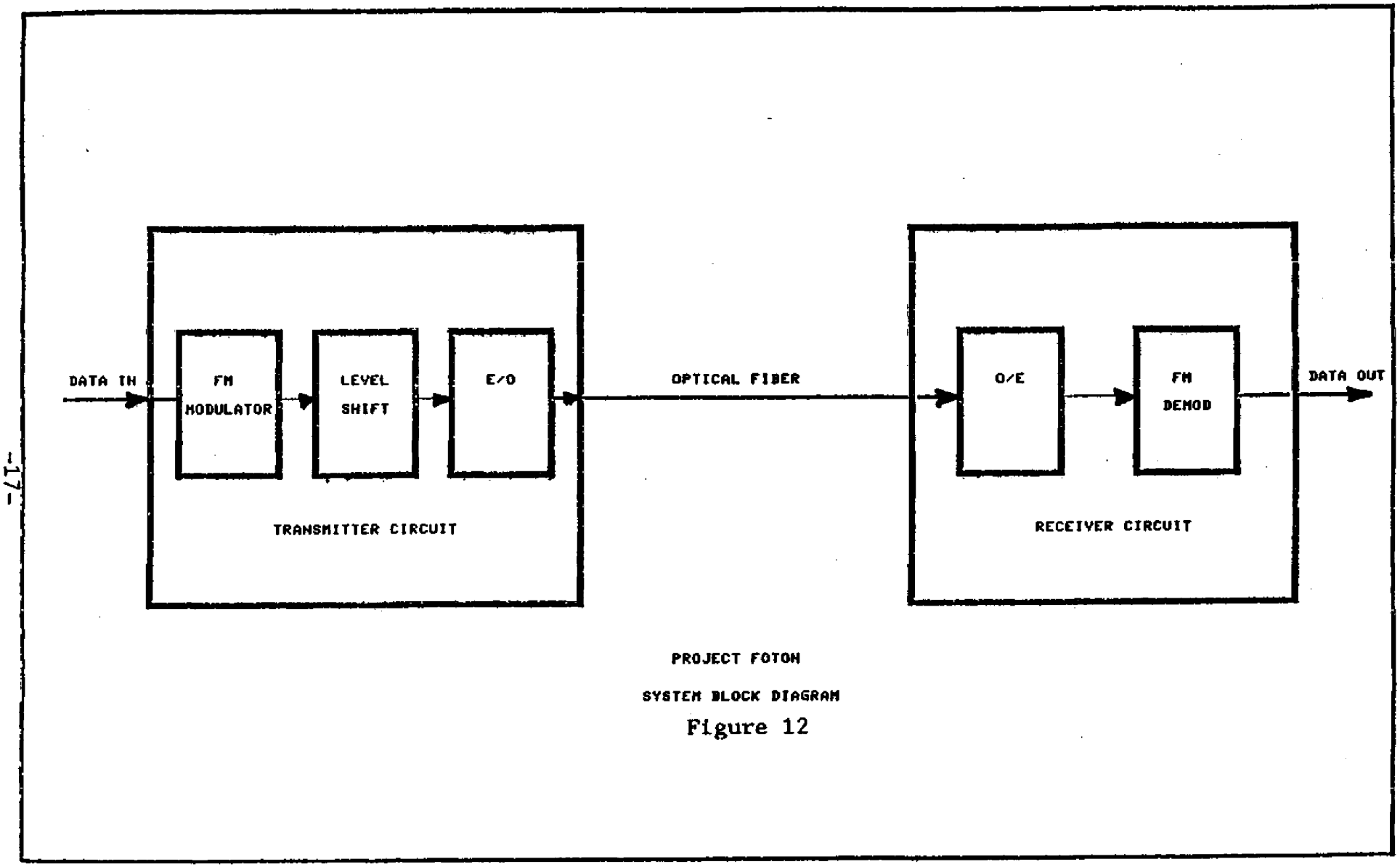
In order to transmit the composite input signal containing the telemetry information as well as the two video signals as they appear in the frequency spectrum layout of Figure 2b, a baseband bandwidth of at least 20 MHz is required. Taking into consideration the tradeoffs discussed in the "FM Theory" section of this report, it was decided to run the VCO at Fc = 125 MHz with a 20% deviation of $\Delta F = \pm 25$ MHz. Thus generating an FM signal with a minimum frequency of 100 MHz and a maximum frequncy of 150 MHz which is the upper limit of the NE-568. The VCO was pushed to its upper limit in order to achieve the largest ΔF and β possible. Using eqns. 2 & 4

$$\beta = 25\text{MHz}/20\text{MHz} = 1.25 \qquad \text{and} \qquad \text{SNR} = 1.5B^2\gamma = 2.34\gamma;$$

therefore this system should theoretically provide a signal to noise ratio 2.34 times greater than that of a baseband communication system becuase of the FM improvement factor.

Figure 14 shows the NE-568 used as a linear frequency modulator. With the exception of pins 4 & 5, all connections on the the left side of the diagram are for power and include an RF choke as well as several bypass capacitors. The capacitor connecting pins 4 and 5 controls the oscillator's free-running frequency and is usually referred to as the timing capacitor Ct. The value of Ct is determined by the desired Fc, the value of the temperature compensation resistor R4, and the amount of stray capacitance on the board. See Appendix C-Figure 6 for correction factors. "Pins 17 and 18 are both biased from Vcc and Vout(pin 14) using R3 and R2. This balanced biasing provides supply rejection and temperature tracking. Capacitor C3 bypasses pin 17 for output signal swings. The RF input (pin 11) is grounded through a 10K resistor in order to drive the internal limiter to a fixed state. Since the internal phase detector multiplies the limiter output and the oscillator signal, the oscillator frequency will appear at the phase detector outputs (pins 19 & 20)." [2] The amplitude of these differential outputs is 200mV pk-pk with a DC offset of Vcc-0.1v. Capacitor Cm is used to control the modulator bandwidth.

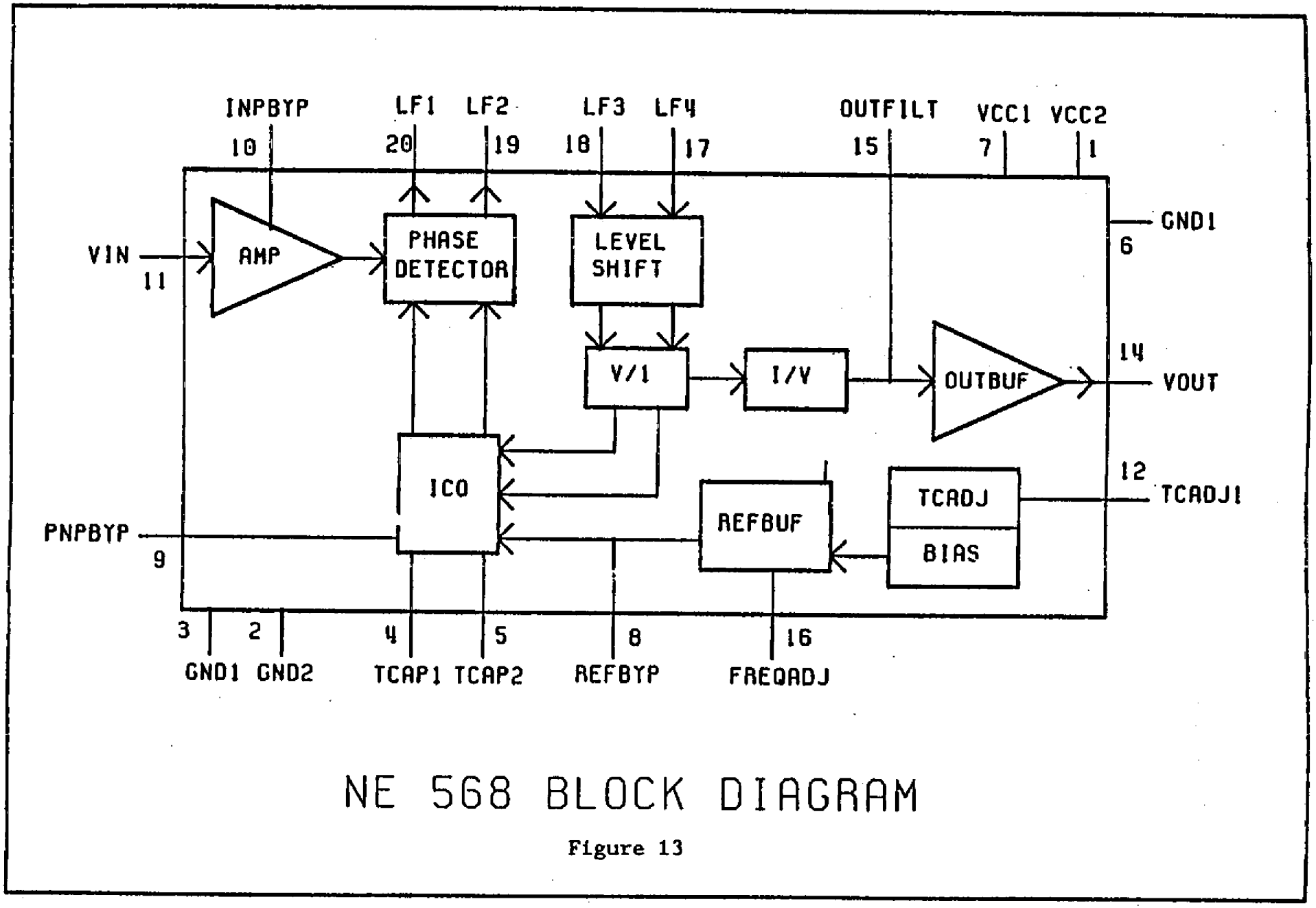
2 - Signetics Corp. Internal Correspondence: "Using the NE-568 as a Frequency Modulator."



PROJECT FOTON

SYSTEM BLOCK DIAGRAM

Figure 12



NE 568 BLOCK DIAGRAM

Figure 13

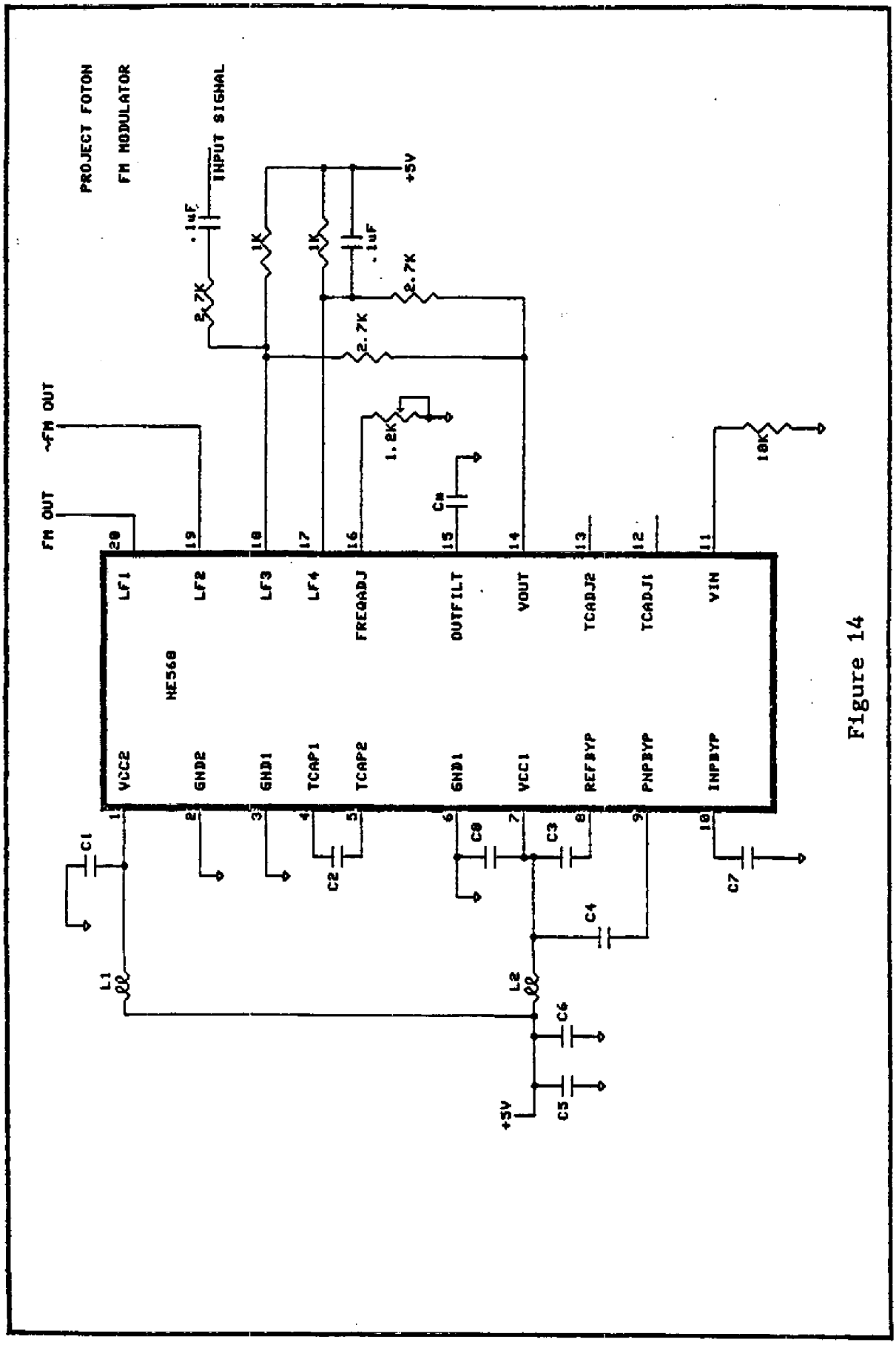

PROJECT FOTON
FM MODULATOR
INPUT SIGNAL
.1uF
1K
1K
.1uF
+5V
2.7K
2.7K
2.7K
~FM OUT
FM OUT
1.2K
C8
18K
LF1
LF2
LF3
LF4
FREQADJ
OUTFILT
VOUT
TCADJ2
TCADJ1
VIN
NE568
VCC2
GND2
GND1
TCAP1
TCAP2
GND1
VCC1
REFBYP
PNPBYP
INPBYP
C1
C2
C8
C3
C4
C7
L1
L2
C6
C5
+5V

Figure 14

The Level Shift/Amp Circuit and E/O Interface

The E/O converter is 100K ECL compatable. This means that its inputs must be at ECL levels which are centered about -1.3V and range from about -1.7V (low) to -0.9V (high), a swing of 800mv. Since the VCO output is 200mV with a DC offset of Vcc-0.1V, it was necessary not only to level shift the signal, but to amplify it by a factor of four as well. This was accomplished through the use of a multi-stage, high bandwidth differential amplifier. This interface was designed differentially because the VCO output is differential and the E/O converter can handle differential inputs as well. It is possible to drive the E/O single-endedly, but it was thought that use of a differential input might improve the signal to noise ratio. The main concern in designing this amplifier/shifter was that there be sufficient bandwidth to handle the modulated signal.

As seen in Figure 15, there are five stages to this amplifier, two gain stages and three emitter follower pairs for buffering. A nice property of the emitter follower circuit is its high input impedance which is used here to ensure that each stage doesn't load down the stage previous to it. Each gain stage is DC coupled to remove any DC offset on the signal. The two gain stages use 2N2369A BJT transistors (T3, T4, T7, and T8 in Figure 15) which have a rated gain bandwidth product (Ft) of about 500MHz. The specification sheets for this device appears in Appendix D. Using the Ic vs Ft curves it was possible to determine the Ic for which the gain bandwidth product was the greatest and bias the transistor appropriately. In this way the bias current for each 2N2369A was chosen as 8mA, or 16mA for each stage. The collector base voltages are also biased to accommodate high bandwidths. The first gain stage has a measured gain of about 2.5 providing a signal large enough to cause the second stage to switch. The second stage is biased so that it will act as an ECL gate. The current switches almost completely between the two legs of the differential pair so that if the diode drop due to the last emitter follower is taken into account, ECL levels are generated at the output of the amplifier.

The amplifier could possibly have been designed in fewer stages but then there would have been potential problems with slew rate, ie. with faster switching there is less chance of noise causing phase error. Thus to avoid this problem, the amplifier/shifter was designed to have a fast switching time requiring several stages since the gain bandwidth product of the

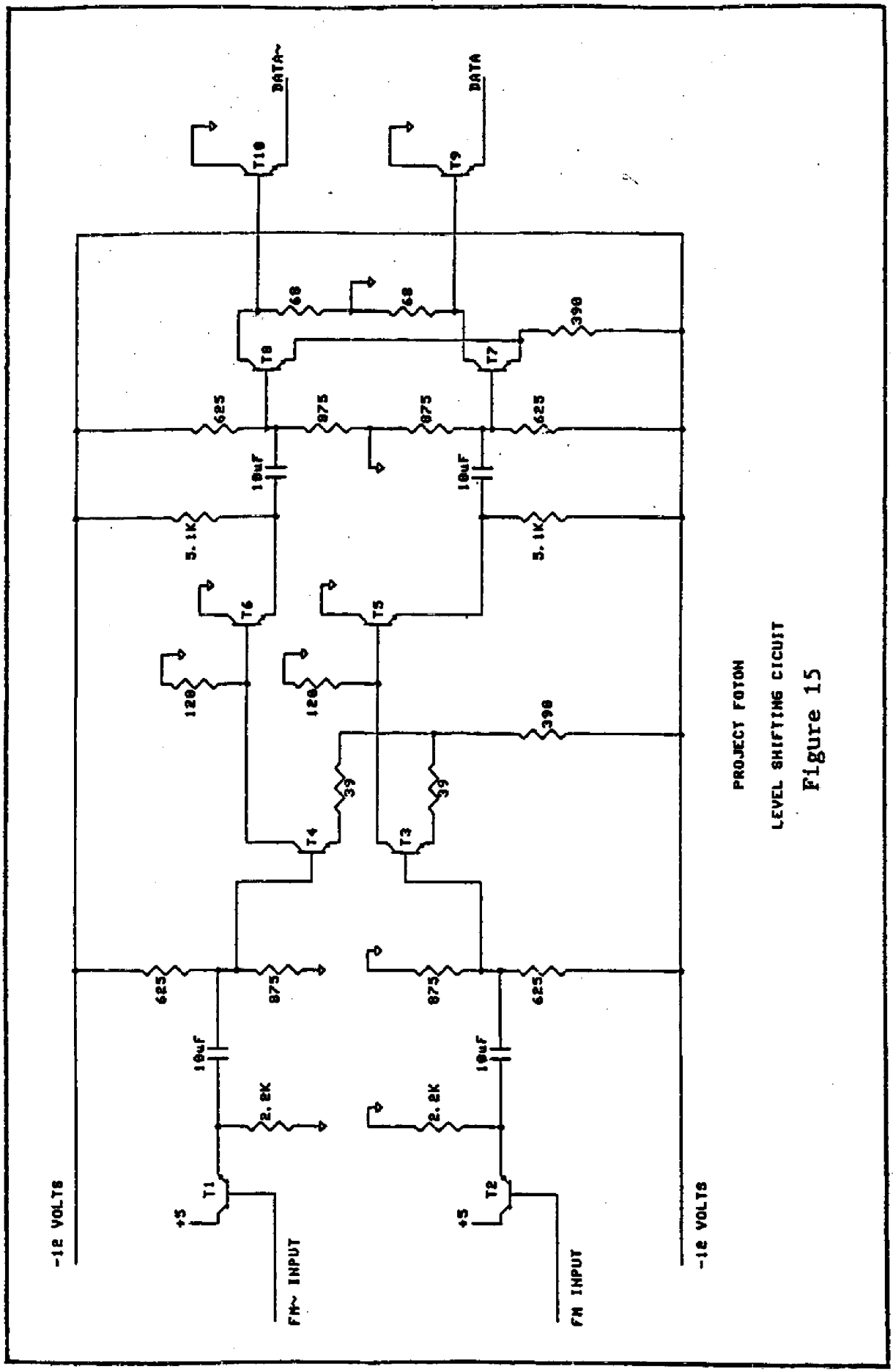

DATA~
DATA
T10
T9
68
68
390
T8
T7
625
875
875
625
10uF
10uF
5.1K
5.1K
T6
T5
120
120
390
39
39
T4
T3
625
875
875
625
10uF
10uF
2.2K
2.2K
T1
T2
+5
+5
-12 VOLTS
-12 VOLTS
FM~ INPUT
FM INPUT
PROJECT FOTON
LEVEL SHIFTING CICUIT

Figure 15

ODL TRANSMITTER AND RECEIVER

The optical components used, as previously mentioned, are the AT&T ODL 1252C (Transmitter) and 1352C (receiver) from the AT&T ODL 200 Lightwave Data Link Kit. The ODL chips, fully compatible with 100K ECL , operate by changing the amplitude of the light emitted from a photodiode. As indicated in the ODL description (see Appendix A), turn-on delay is reduced by biasing the photodiode with a small current in the off position, thus the light in the fiber is never completely off. However, the transmission of data pulses can be thought of as the light being either on or off. This differs from some other methods of optical transmission where instead of modulating the amplitude of the optical signal, the frequency is modulated producing an FSK type of transmission. Connections of the 1252C and 1352C were done as recommended in the specification sheets and are shown in Figures 16 & 17.

THE RECEIVER

The NE-568 Phase Locked Loop

Once the FM signal has been received by the O/E converter, it is fed to the input of the NE-568 PLL shown in Figure 18, through a 0.1uF coupling capacitor. This coupling removes the DC offset of the ECL level output from the O/E converter. The NE-568, which has a center frequency equal to that of the VCO of Fc = 125MHz, "locks on" to the signal as described in the "FM Detection" section earlier in this report. Fc was set using capacitor C2 between pins 4 & 5 as before. All power connections are exactly the same as in the VCO diagram of Figure 14. Other component values were chosen using the specification sheets and diagrams of Appendix C, and equations supplied with the NE-568 documentation. A table of the component values used is included on the circuit diagram.

Since this is a high frequency device, as is the FM modulator, careful attention must be paid toward the layout, mounting, and circuit connection techniques. In the documentation, Signetics Corp. makes it clear that unless certain points are AC bypassed effectively, there is a high probability of extraneous signals being introduced to the signal paths. These bypass capacitors must be ceramic surface mount types which are mounted on the solder side of the board. Also, the NE-568 chip must be soldered in place and Signetics recommended layout (see Figure 19) for the copper traces must be used to ensure satisfactory performance. The FOTON prototype was built paying close attention to these guidelines. Every capacitor on the board is a surface mount type, the NE-568 is soldered in, and the recommended layout for the PLL was used. Trace layouts for all other component connections were designed by the members of FOTON.

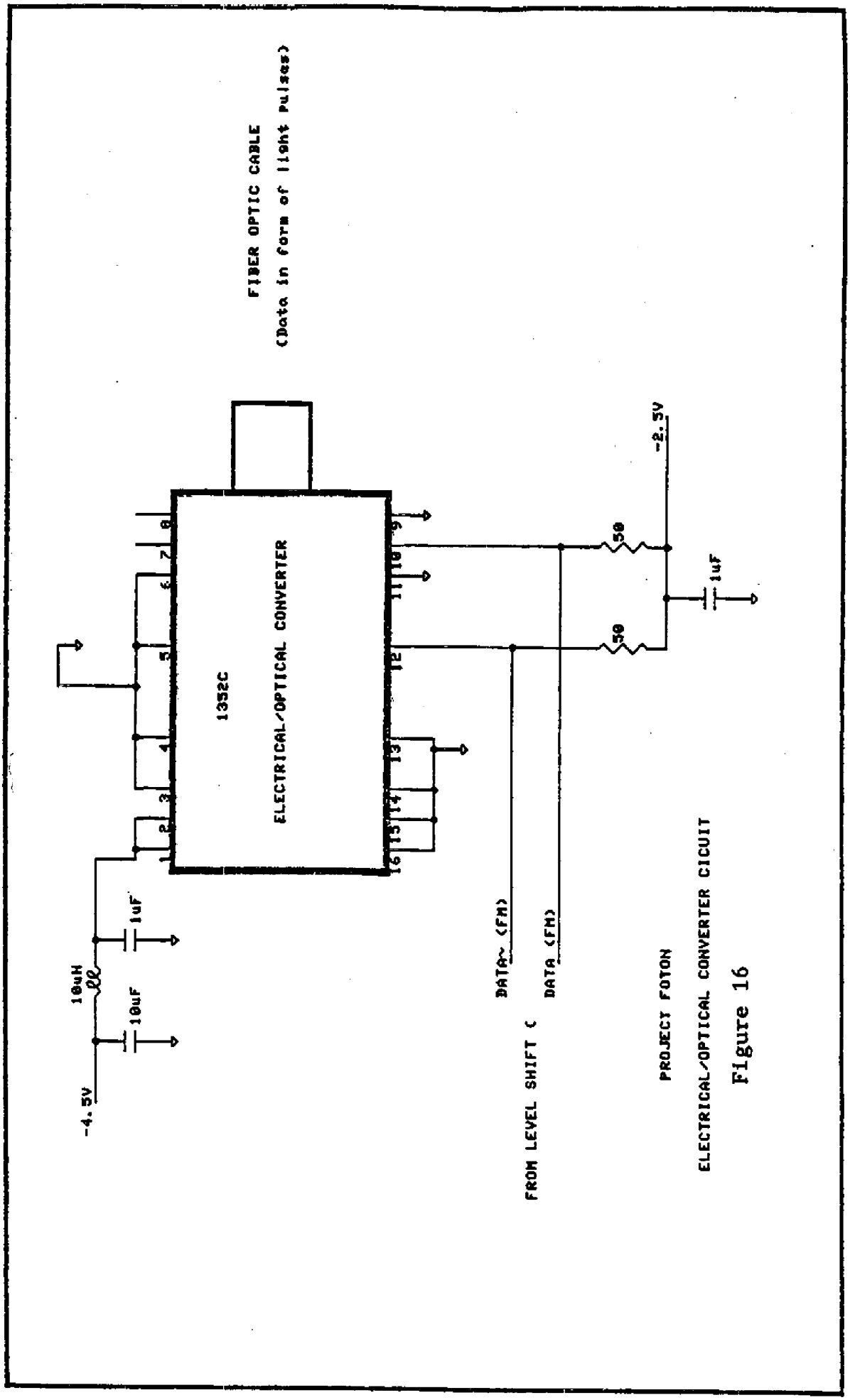

FIBER OPTIC CABLE
(Data in form of light Pulses)
1332C
ELECTRICAL/OPTICAL CONVERTER
-2.5V
50
50
1uF
10uH
10uF
1uF
-4.5V
DATA~ (FM)
DATA (FM)
FROM LEVEL SHIFT C
PROJECT FOTON
ELECTRICAL/OPTICAL CONVERTER CICUIT

Figure 16

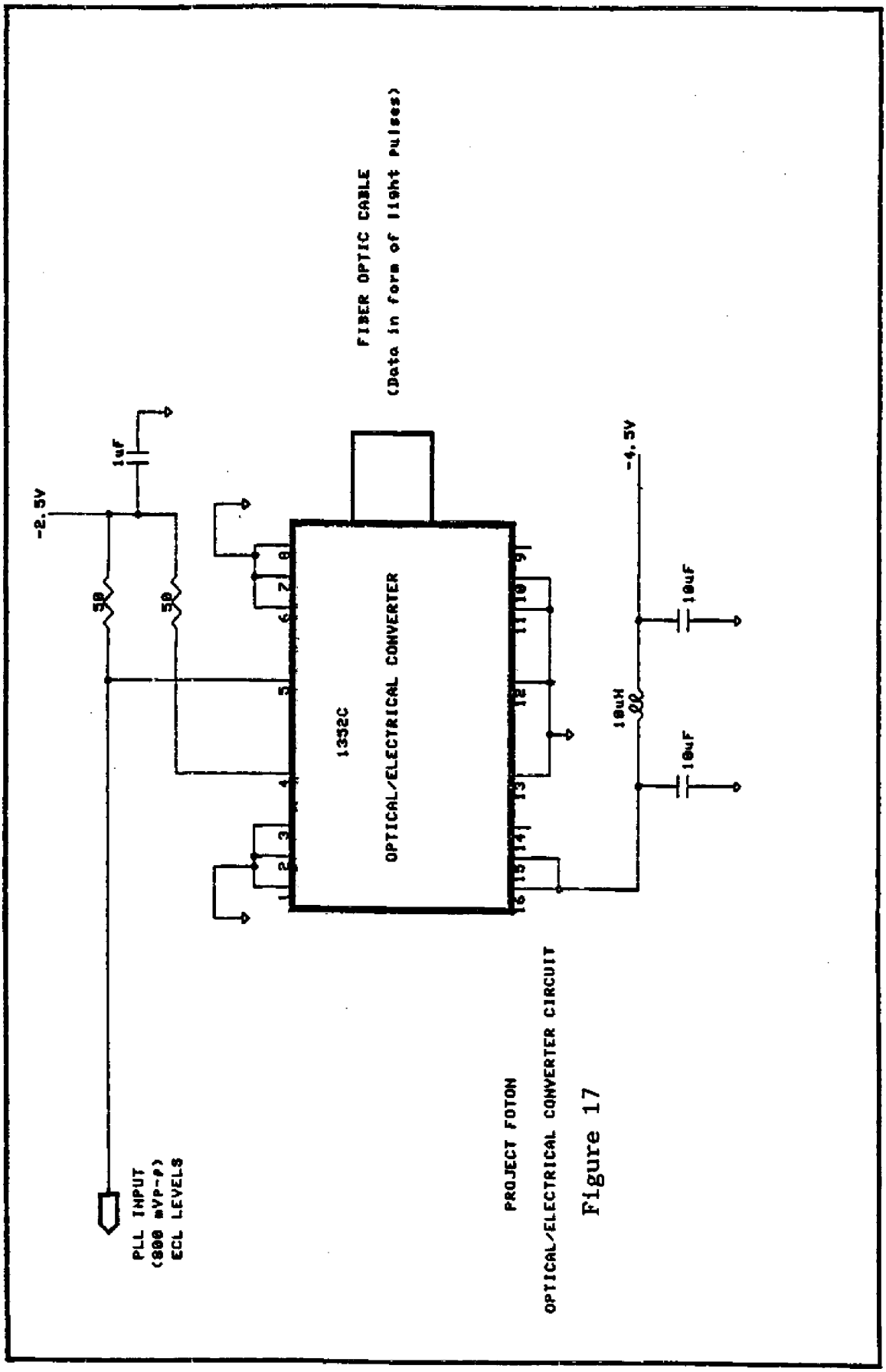

FIBER OPTIC CABLE
(Data in form of light Pulses)
-2.5V
1uF
50
50
1332C
OPTICAL/ELECTRICAL CONVERTER
-4.5V
10uF
10uH
10uF
PLL INPUT
(800 mVp-p)
ECL LEVELS
PROJECT FOTON
OPTICAL/ELECTRICAL CONVERTER CIRCUIT

Figure 17

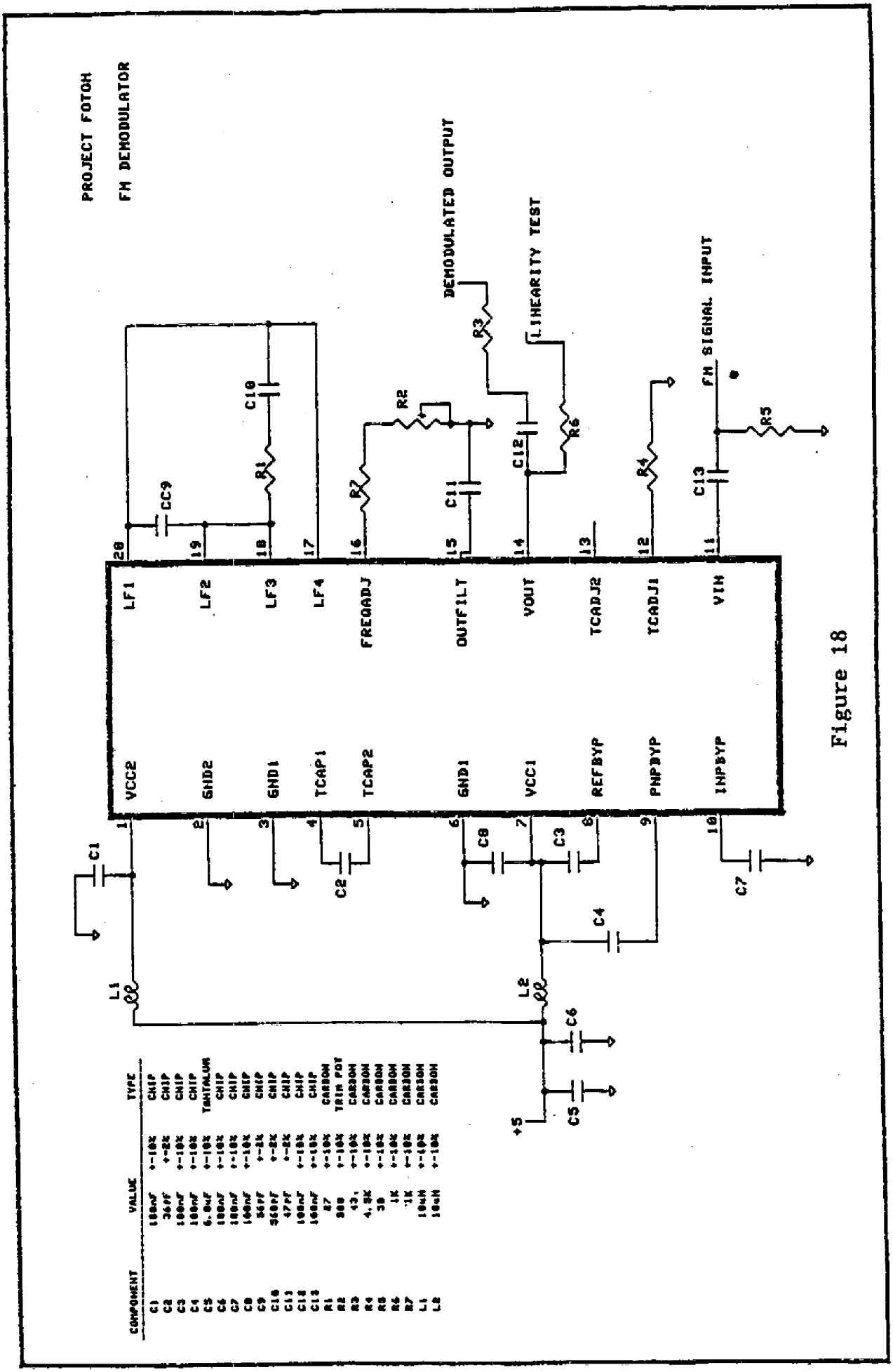

PROJECT FOTOH
FM DEMODULATOR
DEMODULATED OUTPUT
LINEARITY TEST
FM SIGNAL INPUT
LF1
LF2
LF3
LF4
FREQADJ
OUTFILT
VOUT
TCADJ2
TCADJ1
VIN
VCC2
GND2
GND1
TCAP1
TCAP2
GND1
VCC1
REFBYP
PNPBYP
INPBYP
+5
COMPONENT VALUE TYPE
C1 100nF +-10% CHIP
C2 36pF +-2% CHIP
C3 100nF +-10% CHIP
C4 100nF +-10% CHIP
C5 6.8uF +-10% TANTALUM
C6 100nF +-10% CHIP
C7 100nF +-10% CHIP
C8 100nF +-10% CHIP
C9 82pF +-2% CHIP
C10 360pF +-2% CHIP
C11 47pF +-2% CHIP
C12 100nF +-10% CHIP
C13 100nF +-10% CHIP
R1 27 +-10% CARBON
R2 300 +-10% TRIM POT
R3 43, +-10% CARBON
R4 4.3K +-10% CARBON
R5 39 +-10% CARBON
R6 1K +-10% CARBON
R7 1K +-10% CARBON
L1 10uH +-10% CARBON
L2 10uH +-10% CARBON

Figure 18

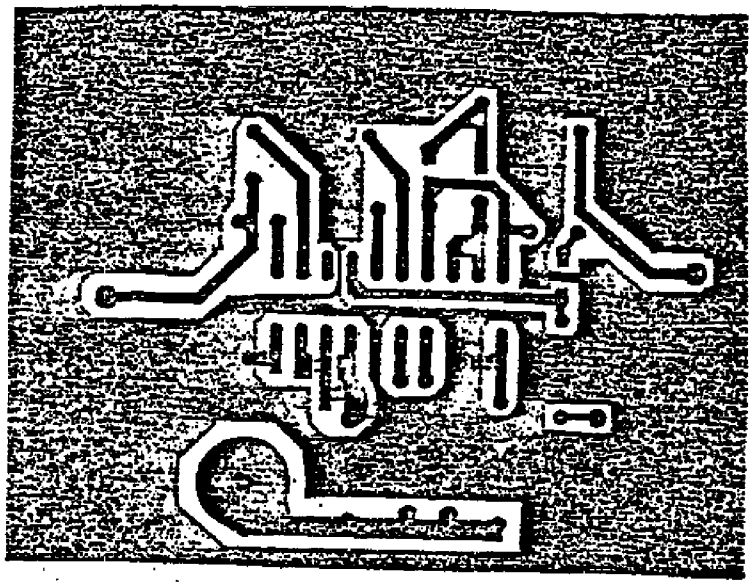


Figure 19 : Suggested Layout for the NE-568

Remixing of Video and Filtering

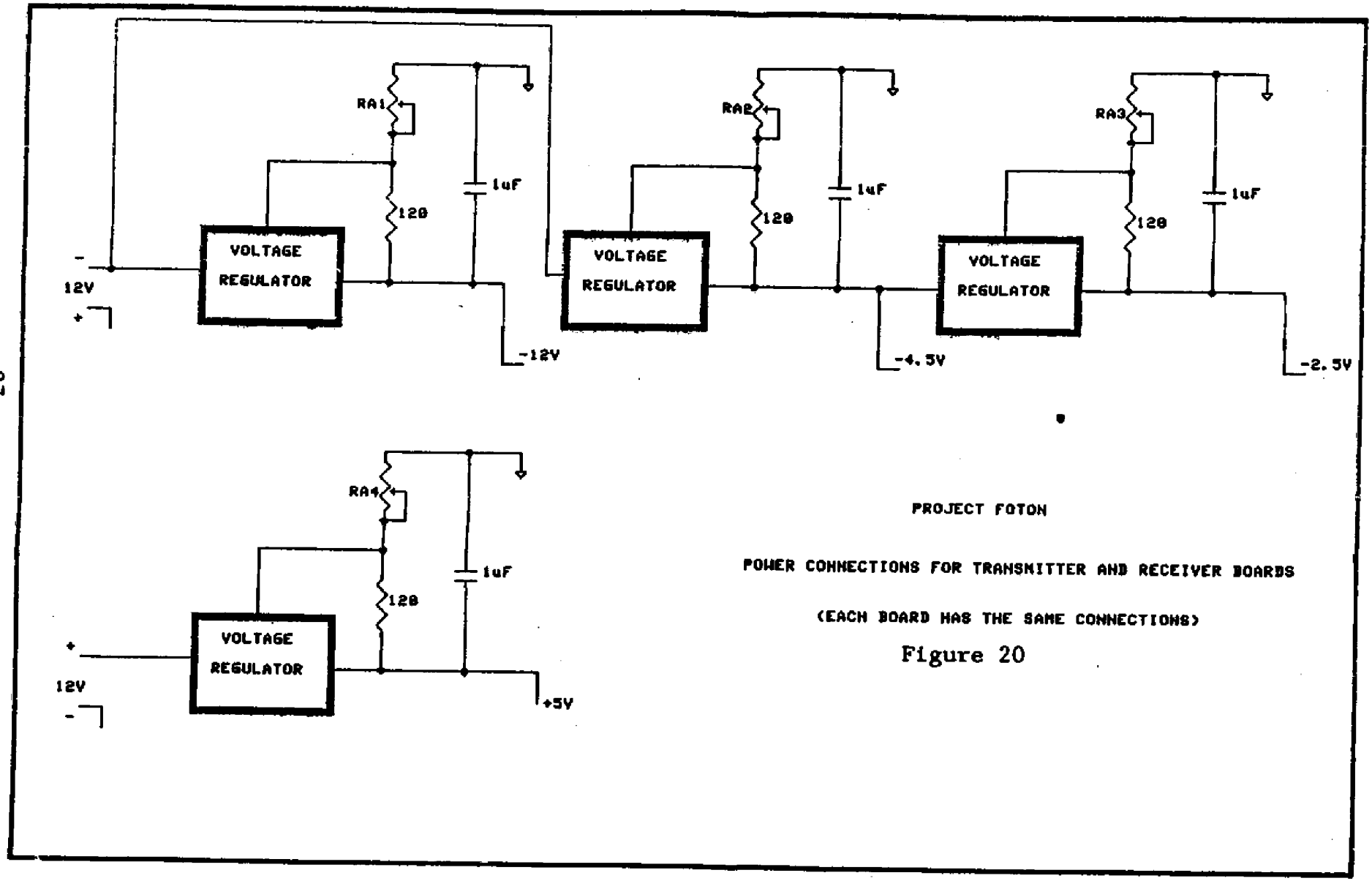
Although not part of FOTON's tasks, any composite signal containing many different parts would have to be filtered and separated after being demodulated by the PLL. If the baseband arrangement of Figure 2b were chosen as the way to organize the three signals, then the system of Figures 4 & 5 could be used to implement it. Whatever arrangement is chosen, it must stay within the 20MHz baseband bandwidth limit.

POWER CONNECTIONS

Voltage levels required for the entire FOTON System include:

Component	Voltage Required
NE-568	+5 Volts
Amplifier/Shifter	-12 Volts
E/O & O/E Converters	-4.5 Volts
	-2.5 Volts

The negative voltages were obtained with a -13.5 volt supply and five NTE-957 adjustable negative voltage regulators. The positive voltages were obtained in the same manner with a +12 volt supply and two NTE-960 positive 5 volt regulators. All power connections are shown in Figure 20. It should be noted that the regulators which supply -4.5 volts to the E/O and O/E converters must supply 260mA and 180mA respectively; therefore these regulators have heat sinks on them to help with heat dissapation.



PROJECT FOTON

POWER CONNECTIONS FOR TRANSMITTER AND RECEIVER BOARDS

(EACH BOARD HAS THE SAME CONNECTIONS)

Figure 20

DEBUGGING

When assembling and testing the system a number of problems arose, the more serious of which will be summarized here. The first time the system worked, an inversion of the signal was observed. This was caused by the VCO having a negative transfer function with respect to the PLL's transfer function. That is, the output frequency of the VCO increased for negative input voltage levels and decreased for positive input voltages. This problem was easily solved by flipping the differential input leads (pins 17 & 18) to the VCO circuit. Now a positive input voltage to the VCO corresponds to an increase in oscillator frequency and vice-versa.

Another major problem resulted from a large amount of noise getting onto the traces through the power supplies. The effect of this noise was observable interference in the video signal. The noise was pinpointed with an oscilliscope and the problem alleviated by placing 10uF capacitors from the supply side of the positive voltage regulators to ground.

Other problems included bad capacitors that acted as short circuits and bad solder joint which created open circuits. It was also discovered that the input signal to the VCO can't exceed much more than 0.5 volts pk-pk without distorting the signal. Therefore, a simple voltage divider was built at the input with a potentiometer so that the input signal level could be adjusted to appropriate levels.

Appendix A

AT&T ODL 200 Lightwave Data Link Specifications

AT&T
ODL 200 LIGHTWAVE DATA LINK MODELS KIT INSTRUCTION MANUAL

December 1985

INTRODUCTION

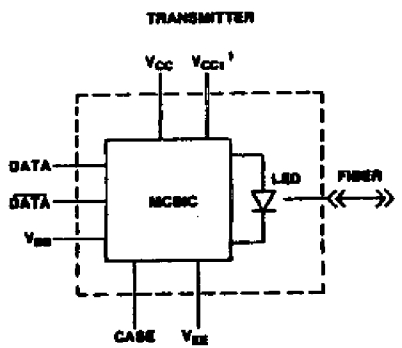
The AT&T *ODL* 200 Lightwave Data Link Models Kit provides a means to investigate the benefits and performance of our latest lightwave data link product. The kit includes a 1252C Transmitter module, a 1352C Receiver module, and 50 feet of 62.5/125μm connectorized lightguide cable. This Instruction Manual provides an overview of the basic components and information helpful in applying fundamental applications of the lightwave data link.

BASIC COMPONENTS IN THE *ODL* 200 LIGHTWAVE DATA LINK MODELS KIT

Transmitter

The 1252C Transmitter is designed for data rates up to 220 Mb/s (NRZ) and provides −19 dBm peak power output. To achieve these high data rates, the transmitter uses microwave complementary bipolar integrated circuit (MCBIC) technology. It operates from either a +4.5 volt (+ Vcc) or a −4.5 volt (− VEE) power supply with a maximum supply current of 260 mA and is mounted in a 16-pin dual in-line package (DIP). The metal DIP should be grounded to provide a high degree of EMI/RFI protection. The integral lens-coupled optical connector used by the transmitter mates with an AT&T *ST*™ Series Multimode Fiber Optic Connector.

In addition to a long-wavelength, high-speed light-emitting diode (LED), the transmitter consists of a silicon integrated circuit and several discrete components. The transmitter is fully compatible with 100K ECL input data and produces binary 1320 nm optical output signals. All driver and bias circuits for the transmitter's InGaAsP high-radiance LED are included in the transmitter package (Figure 1). To minimize turn-on delay, the LED is biased at a small current in the off condition.



Note 1. V_{CC1} — LED Supply Voltage normally not equal to V_{CC}.

Figure 1

Differential data is the normal input signal; however, single-ended signals can be used by connecting pin 8 (V_{EE}) to the unused data input or $\overline{data}$ input (pin 10 or 12, respectively). Pin locations are shown in Figure 2.

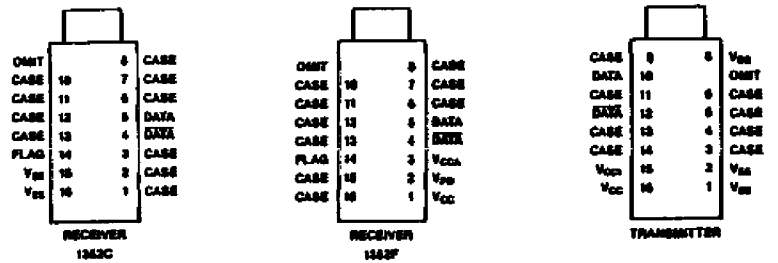
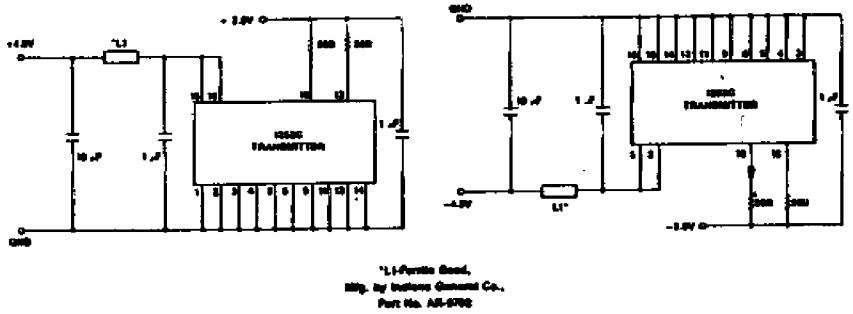


Figure 2

A recommended wiring schematic for the 1252C transmitter is indicated in Figures 3A and 3B. A maximum case temperature of 70°C is suggested. The user should utilize a sound microwave wiring layout technique and provide a ground plane on the component side of the printed wiring board, under the module. The use of sockets is detrimental. Bypass components should be located as close to the module as possible.



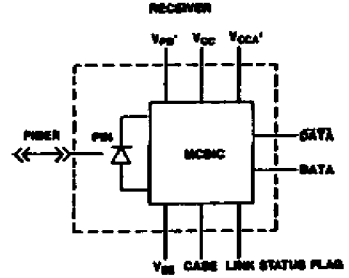
*L1-Ferrite Bead,

Figure 3A

Figure 3B

Receiver

The 1352C Receiver, shown in Figure 4, includes circuit technology similar to that in the 1252C Transmitter. The design consists of a transimpedance preamplifier following the PIN photodiode, a postamplifier, decision circuits, and logic output stages. The PIN photodetector diode provides the receiver with an overall peak power sensitivity of −29 dBm at a bit error rate of 10^{-9}. The receiver is designed to operate for data rates up to 220 Mb/s.

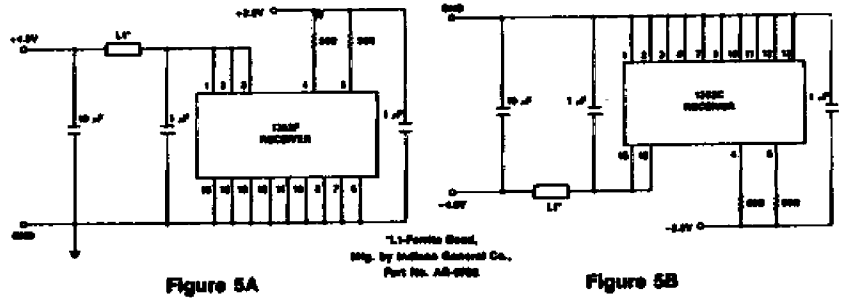


Notes: 1. V_{PD} – Photodiode Supply Voltage normally set equal to V_{CC}.
2. V_{CCA} – Positive Supply Voltage for Output Logic Stages.

Figure 4

The 1352F receiver requires a +4.5 volt (+V_{CC}) power supply and the 1352C receiver a −4.5 volt (−V_{EE}) power supply. Both operate with a maximum current of 150 mA. A maximum case temperature of 70°C is suggested. A recommended wiring schematic for each receiver is indicated in Figures 5A and 5B. The user should utilize a sound microwave wiring layout technique and provide a ground plane on the component side of the printed wiring board, under the module. The use of sockets is detrimental. Bypass components should be located as close to the module as possible.

To maintain maximum sensitivity, the negative supply must be quiet electrically with respect to ground, which is helped by the recommended filtering. Regardless of the amplitude of the power supply noise voltage, the slew rate (dV/dT) at the V_{EE} pins (pins 15 and 16, Figure 5B) should be less than 0.25 V/μs.



*L1-Ferrite Bead,

Figure 5A

Figure 5B

ELECTRICAL CHARACTERISTICS

ODL 200 Receiver

(V_{CC} [1352F] – V_{EE} [1352C][1] = 4.2 to 4.8 V; Operating Temperature: 0 to 70°C[1])
(Complementary Outputs[2])

Parameter	Symbol	Min	Max	Unit
Output Data Voltage—Low[3,4] Output Data Voltage—Low[3]	V_{OL} V_{OL}	−1.810 −1.830	−1.620 −1.605	V V
Output Data Voltage—High[3,4] Output Data Voltage—High[3]	V_{OH} V_{OH}	−1.025 −1.035	−0.880 −0.870	V V
Current Drain on V_{CC}	I_{CC}	–	150	mA
Current Drain on V_{PD}	I_{PD}	–	75	μA
Current Drain on V_{CCA}[5]	I_{CCA}	–	30	mA
Data Rate [NRZ Encoding]	DR	40	220	Mb/s
Optical Sensitivity—Typical Operating Conditions[6] Optical Sensitivity—Worst Case[7]	P_{IN} P_{IN}	0.8 (−31) 1.1 (−29.5)	– –	μW (dBm) μW (dBm)
Maximum Input Power	P_{MAX}	–	88 (−10.5)	μW (dBm)
Optical Wavelength for Rated Sensitivity	λ	1275	1375	nm
Pulse Width Distortion[8,9]	PWD	–	1.2	ns
Output Rise Time[9,10] Output Fall Time[9,10]	t_R t_F	– –	1.4 1.4	ns ns
Power Dissipation[11]	P_{DISS}	–	.750	W
Flag—Low[12] Flag—High[12]	V_{FL} V_{FH}	−1.830 −1.035	−1.605 −0.870	V V

NOTES:

1. Refer to thermal characteristics, p. 5.
2. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved using either output individually.
3. The 1352C is measured from ground with a 50 Ω load to −2.0 V. The 1352F is measured from V_{CCA} with a 50 Ω load to V_{CCA} −2.0 V.
4. With a 4.5 V power supply.
5. With 50 Ω loads on Data and $\overline{\text{Data}}$ to [V_{CC} −2.0] V (1352F), to −2.0 V (1352C).
6. Value given is typical, not minimum.
7. Peak power coupled from a 0.29 NA, 62.5/125 micron fiber at 220 Mb/s for a bit error rate of 10^{-9} at +40°C. Includes EOL.
8. The PWD as measured with a −18 dBm input signal having negligible PWD.
9. Specified at a 200 Mb/s data rate. At lower data rates the maximum value scales inversely with the decrease in data rate.
10. Between 20% and 80% points with a 50 Ω load to [V_{CC} −2.0] V.
11. With 4.8 V power supply, 50% duty cycle and logic outputs terminated in 50 Ω to V_{CC} −2 V.
12. Measured from V_{CC} with a 50 Ω load to [V_{CC} −2.0] V.

ELECTRICAL CHARACTERISTICS

ODL 200 Transmitter

(V_{CC} – V_{EE} = 4.2 to 4.8 V; Operating Temperature: 0 to 70°C[1])
(Complementary Inputs[2])

Parameter	Symbol	Min	Max	Unit
Input Data Voltage—Low[3] Input Data Voltage—High[3]	V_{IL} V_{IH}	−1.810 −1.165	−1.475 −0.880	−1.7 V V
Input Current—Low[4] Input Current—High[5]	I_{IL} I_{IH}	0.5 –	– 0.350	μA mA
Reference Voltage[6]	V_{BB}	−1.396	−1.244	V
Input Transition Time[7,8]	T_{IN}	–	1.0	ns
Power Supply Current	I_{CC}	–	260	mA
Data Rate [NRZ Encoding]	DR	40	220	Mb/s
Peak Optical Power (Typical Conditions[9])	P_{OH}	28 (−15.5)	–	μW (dBm)
Optical Output[10] High Low	P_{OH} P_{OL}	12.5 (−19) –	88 (−10.5) $P_{OH}/20$ (P_{OH} −13)	μW (dBm) μW (dBm)
Output Rise Time[7,8] Output Fall Time[7,8]	t_R t_F	– –	1.8 2.2	ns ns
Pulse Width Distortion[8,11]	PWD	–	0.5	ns
Optical Wavelength	λ	1300	1350	nm
Spectral Width [FWHM]	Δλ	–	170	nm
Power Dissipation[12]	P_{DISS}	–	1.3	W

NOTES:

1. Refer to package thermal characteristics, p. 3.
2. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-ended.
3. Measured from V_{CC} with a 50 Ω load to [V_{CC} −2.0] V.
4. Measured with V_{IL} min.
5. Measured with V_{IH} max.
6. Measured from V_{CC}.
7. Between 10% and 90% points.
8. Specified at a 200 Mb/s data rate. At lower data rates the maximum value scales inversely with the decrease in data rate.
9. Value given is typical, not minimum.
10. Measured peak power coupled into 0.29 NA, 62.5/125 micron fiber at +40°C. Includes power supply and end-of-life (EOL) variations.
11. The PWD as measured with an input signal having negligible PWD.
12. With 4.8 V power supply and 50% duty cycle.

Appendix B

Exar XR-215 35 MHz PLL Specifications

XR-215

Monolithic Phase-Locked Loop

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single external capacitor. The operational amplifier can be used for audio preamplification in FM detector applications; or, as a high speed sense amplifier (or comparator) in FSK demodulation.

FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility
Wide Dynamic Range: 300 μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal Controlled Detection
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

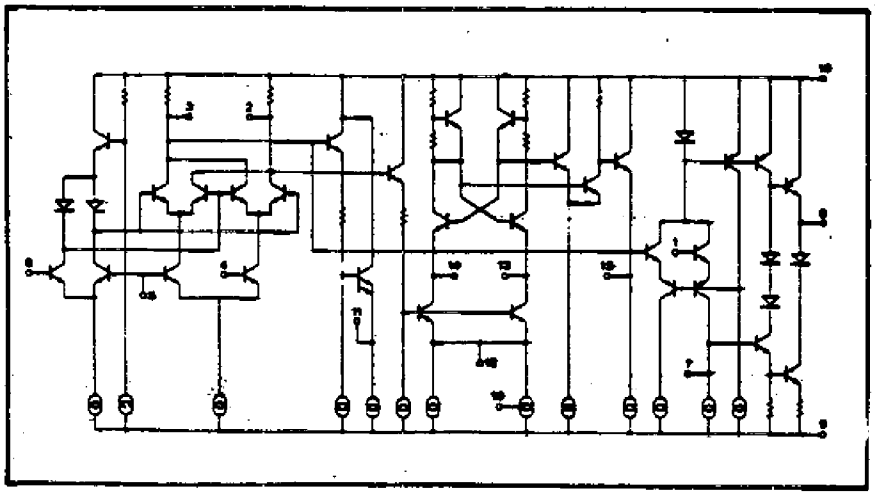
ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation	750 mW
Derate above +25°C	5 mW/°C
Temperature	
Storage	−65°C to +150°C

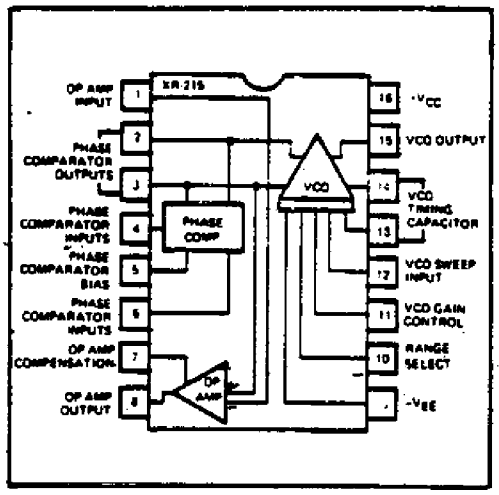
AVAILABLE TYPE

Part Number	Package	Operating Temperature
XR-215CN	Ceramic	0°C to 75°C

EQUIVALENT SCHEMATIC



FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

CHARACTERISTICS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
I – GENERAL CHARACTERISTICS Test Conditions: V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.					
SUPPLY VOLTAGE					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500 µF
VCO SECTION:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 2, $0°C \leq T_A \leq 75°C$
Power Supply		0.1		%/V	$V^+ > 10V$
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$ See Figure 9, C_0 = 2000 pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	10 pF to ground at Pin 15
Fall Time		20		ns	
PHASE COMPARATOR SECTION:					
Conversion Gain		2		V/rad	$V_{in} > 50$ mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3 V_{in} = 0, S_5 open
OP AMP SECTION:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/µsec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		V_{p-p}	R_L = 30 kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II – SPECIAL APPLICATIONS **A) FM Demodulation** Test Conditions: Test circuit of Figure 4, V^+ = 12V, input signal = 10.7 MHz FM with Δf = 75 kHz, f_{mod} = 1 kHz.					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude	250	500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{in} = 10 mV rms, 30% AM
Output Signal/Noise	55	65		dB	
B) Tracking Filter Test Conditions: Test circuit of Figure 5, V^+ = 12V, f_o = 1 MHz, V_{in} = 100 mV rms, 50Ω source.					
Tracking Range (% of f_O)	±30	±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{out}}{\Delta f/f_o}$		50		mV/%	Adjustable – See applications information

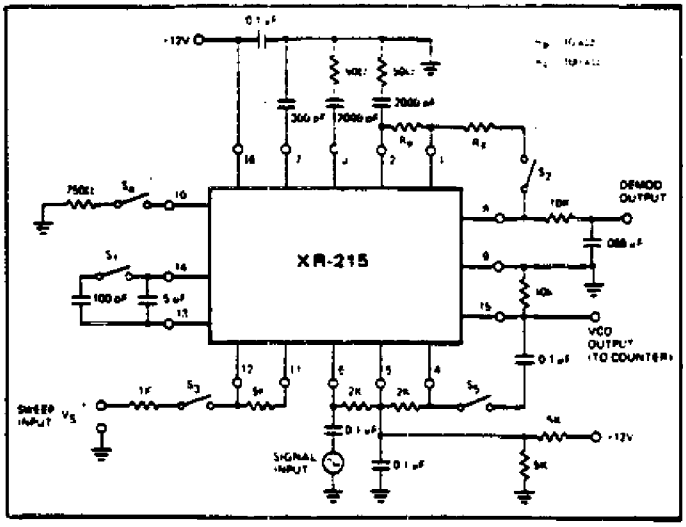


Figure 2. Test Circuit For Single Supply Operation

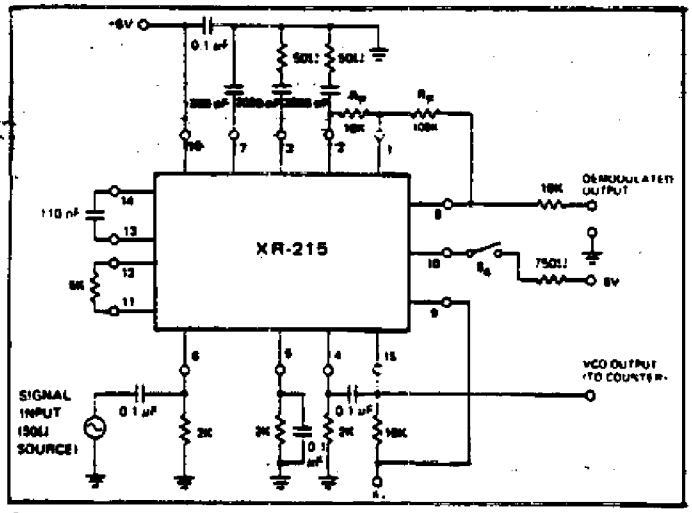


Figure 3. Test Circuit For Split-Supply Operation

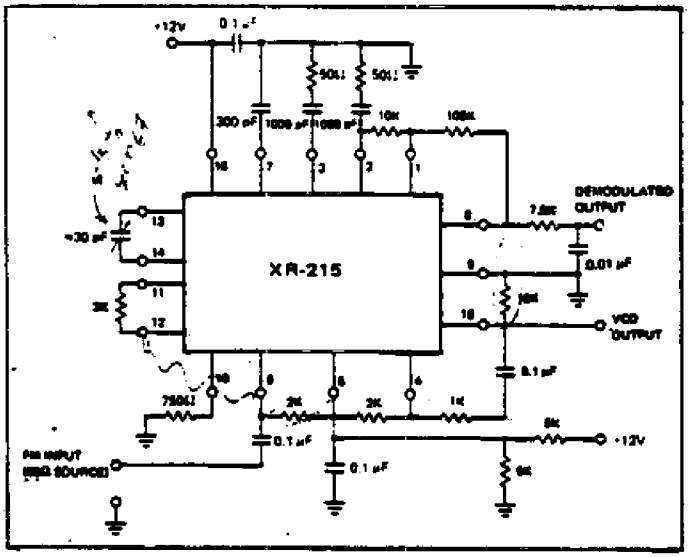


Figure 4. Test Circuit For FM Demodulation

DESCRIPTION OF CIRCUIT CONTROLS

PHASE COMPARATOR INPUTS (PINS 4 AND 6)

One input to the phase comparator is used as the signal input; the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 2). For split supply operation, these inputs are biased from ground as shown in Figure 3. For single supply operation, a resistive bias string similar to that shown in Figure 2 should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8 μA.

PHASE COMPARATOR BIAS (PIN 5)

This terminal should be dc biased as shown in Figures 2 and 3, and ac grounded with a bypass capacitor.

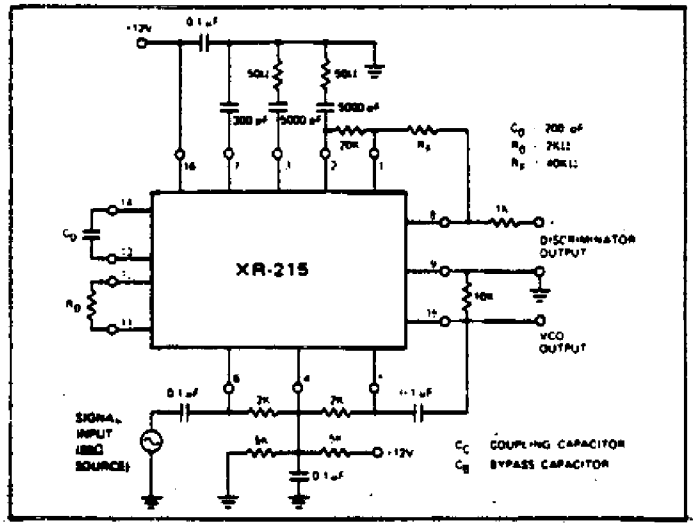


Figure 5. Test Circuit For Tracking Filter

PHASE COMPARATOR OUTPUTS (PINS 2 AND 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see Figure 1). One of the outputs (pin 3) is internally connected to the *non-inverting* input of the operational amplifier. The low-pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in Figure 14.

VCO TIMING CAPACITOR (PINS 13 AND 14)

The VCO free-running frequency, f_0, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See Figure 7).

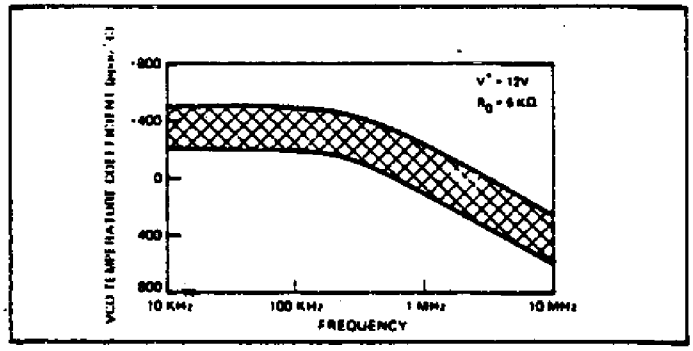


Figure 6. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (pin 10 open)

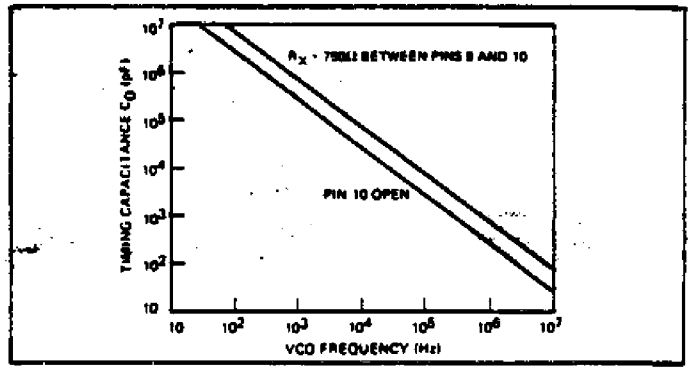


Figure 7. VCO Free Running Frequency vs Timing Capacitor

VCO OUTPUT (PIN 15)

The VCO produces approximately a 2.5 V_{p-p} output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10 kΩ resistor to increase the output current drive capability. For high voltage operation (V_{CC} > 20V), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

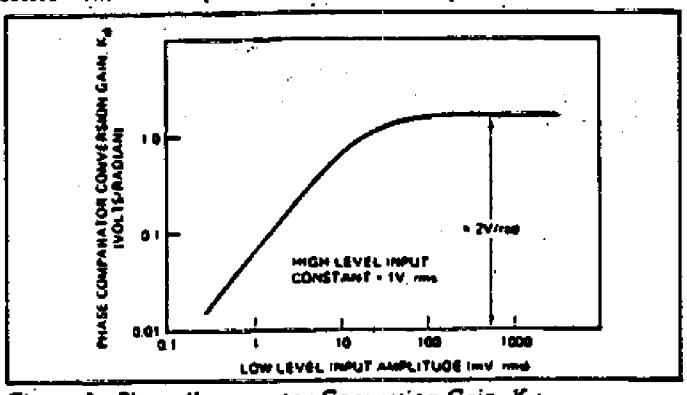


Figure 8. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

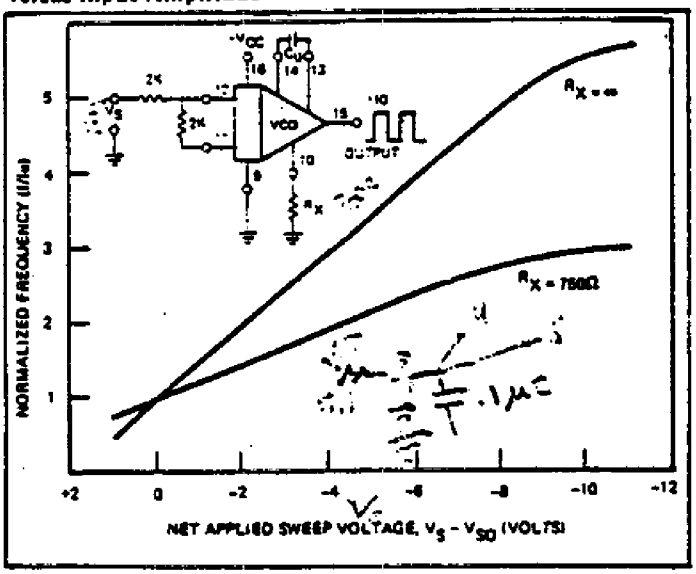


Figure 9. Typical Frequency Sweep Characteristics as a Function of Applied Sweep Voltage

(Note: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

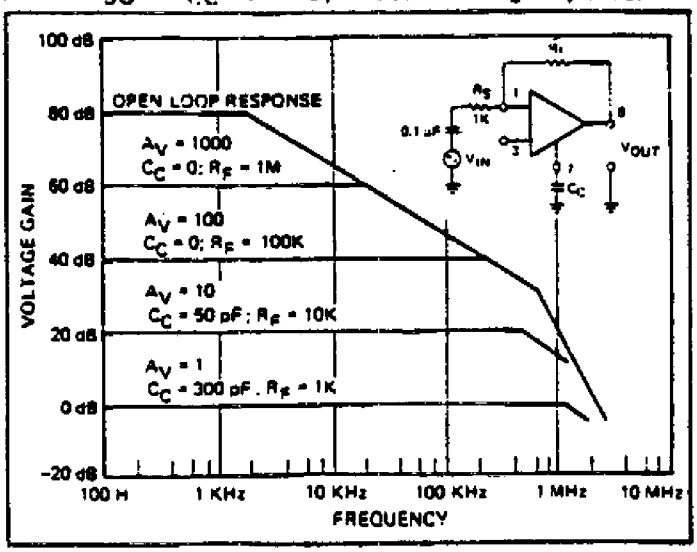


Figure 10 XR-215 Op Amp Frequency Response

VCO SWEEP INPUT (PIN 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 9). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 9. The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less under all operating conditions.

ON-OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open-circuit value. When sweep, sync, or on-off keying functions are not used, R_S should be left open circuited.

RANGE-SELECT (PIN 10)

The frequency range of the XR-215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to Figure 11, the operation of the range-select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_o = f_1 \left(1 + \frac{0.6}{R_X}\right)$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X (≈ 750Ω) is recommended for operation at frequencies in excess of 5 MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

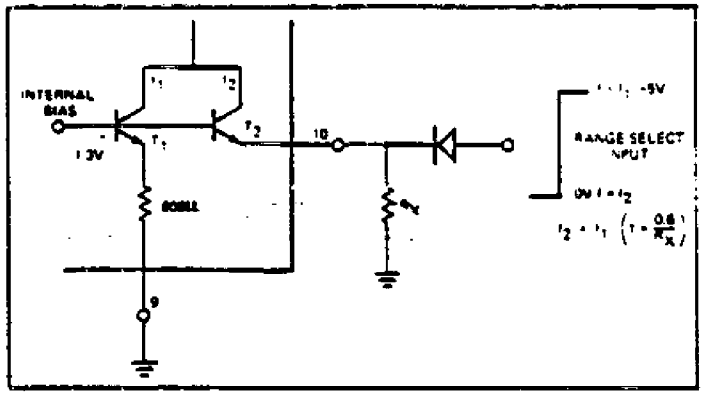


Figure 11 Explanation of VCO Range-Select Controls

DIGITAL PROGRAMMING

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in Figure 11. For high level logic inputs, transistor T_2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR-215 can be time-multiplexed between two separate input frequencies, as shown in Figures 18 and 19.

AMPLIFIER INPUT (PIN 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see Figure 2 or 3).

Appendix C

Signetics NE-568 150 MHz PLL Specifications

150 MHz PLL Preliminary Specification

DESCRIPTION

The NE568 is a Monolithic Phase Lock Loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current controlled oscillator (ICO), a phase detector, level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate +/- 20% deviations with less than 4.0% nonlinearity (1.0% typical). In addition to high linearity the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20 lead dual-in-line and 20 lead SO (surface mounted) plastic packages.

FEATURES

- o Operation to 150MHz
- o High linearity buffered output
- o Series or shunt loop filter component capability
- o Temperature compensated

APPLICATIONS

- o Satellite receivers
- o Fiber optic video links
- o VHF FSK demodulators

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
	Junction temperature	+150	°C
T_{STG}	Storage temperature	-65 to +150	°C
P_{Dmax}	Maximum power dissipation	500	mW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
Plastic 20-Pin DIP	0 TO +70°C	NE568N
Plastic 20-Pin SO Package	0 TO +70°C	NE568D

Electrical Characteristics

The electrical characteristics listed below are actual tests (unless otherwise stated) performed with an automatic IC tester on each device prior to shipment. Performance of the device in an automated test setup is not necessarily optimum. The NE568 is layout sensitive. Evaluation of performance for correlation to the datasheet should be done with the circuit and layout of Figures 1-3 with the evaluation unit soldered in place (do not use a socket!).

TEST CONDITIONS, unless otherwise specified: T_A = 25°C; V_{CC} = 5V; f_0 = 70MHz; Test Circuit - Figure 1; f_{IN} = -20dBm.

DC Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC} supply voltage		4.75	5	5.25	V
Supply current			60	75	mA

AC Electrical Characteristics

Maximum oscillator operating frequency [3]		150			MHz
Input signal level		50 -20 (1)		2000 + 1010	mVp-p dBm
Demodulated BW			$F_0/7$		MHz
Non-Linearity [5]	Dev = ±20%, Input -20dBm		1.0	4.0	%
Lock range [2]	Input -20dBm	±25	±35		% of f_0
Capture range [2]	Input -20dBm	±20	±30		% of f_0
TC of f_0	FIG 1		100		PPM /°C
Input resistance [4]		1K			ohms
Output impedance			6		ohms
Demodulated V_{OUT}	Dev = ±20% of F_0 measured at Pin 4	.40	.50		Vp-p
AM rejection	V_{in} = -20dBm (30% AM) referred to ± 20% deviation		45		dB

f_0 Distribution [6]	Centered at 70MHz, R_2=1.2k	-15	0	+15	%
f_0 Drift with supply	4.75V to 5.25V		1		%/V

Notes:

1 Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.

2 Limits are set symmetrical to F_0. Actual characteristics may have asymmetry beyond the specified limits.

3 Not 100% tested, but guaranteed by design.

4 Input impedence depends on package capacitance. See Figures 4 and 5.

5 Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated based on variance between the measured DC values and an extrapolation of a "Best Fit" straight line over th deviation range specified.

6 Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

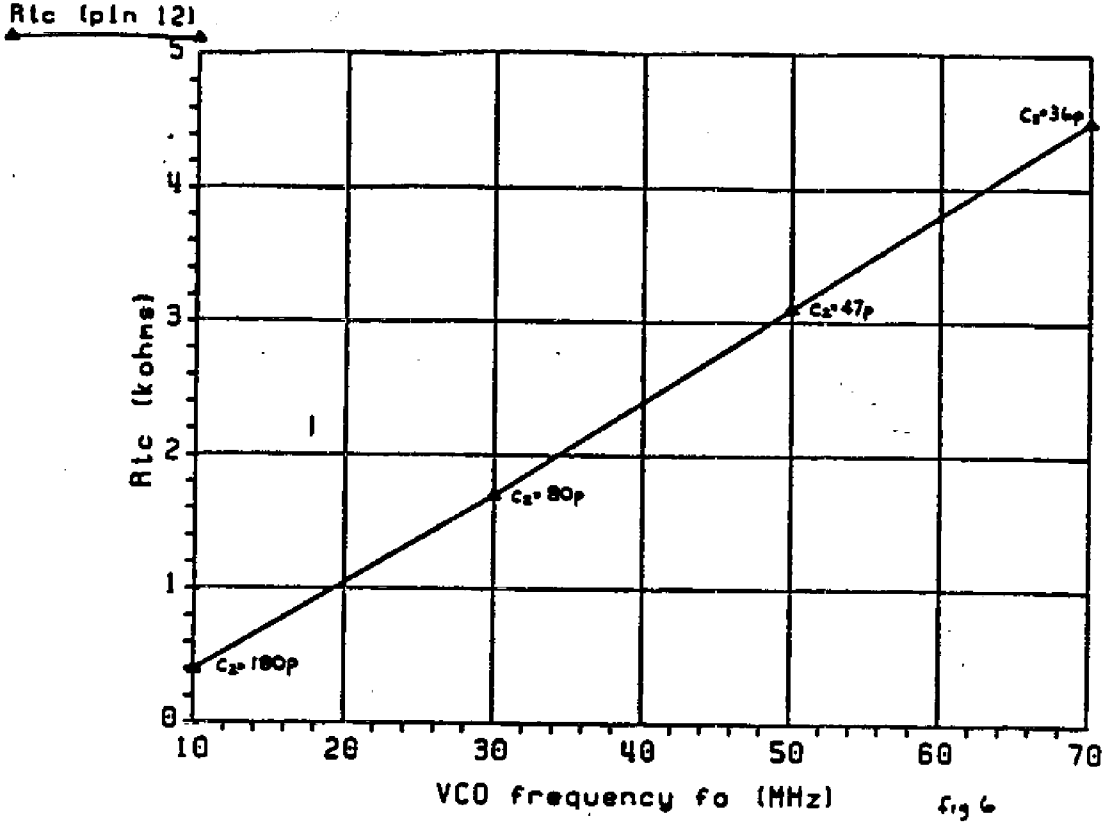

Rtc (pin 12)
Rtc (kohms)
0
1
2
3
4
5
10
20
30
40
50
60
70
VCO frequency fo (MHz)
C_2=180p
C_2=80p
C_2=47p
C_2=36p

fig 6

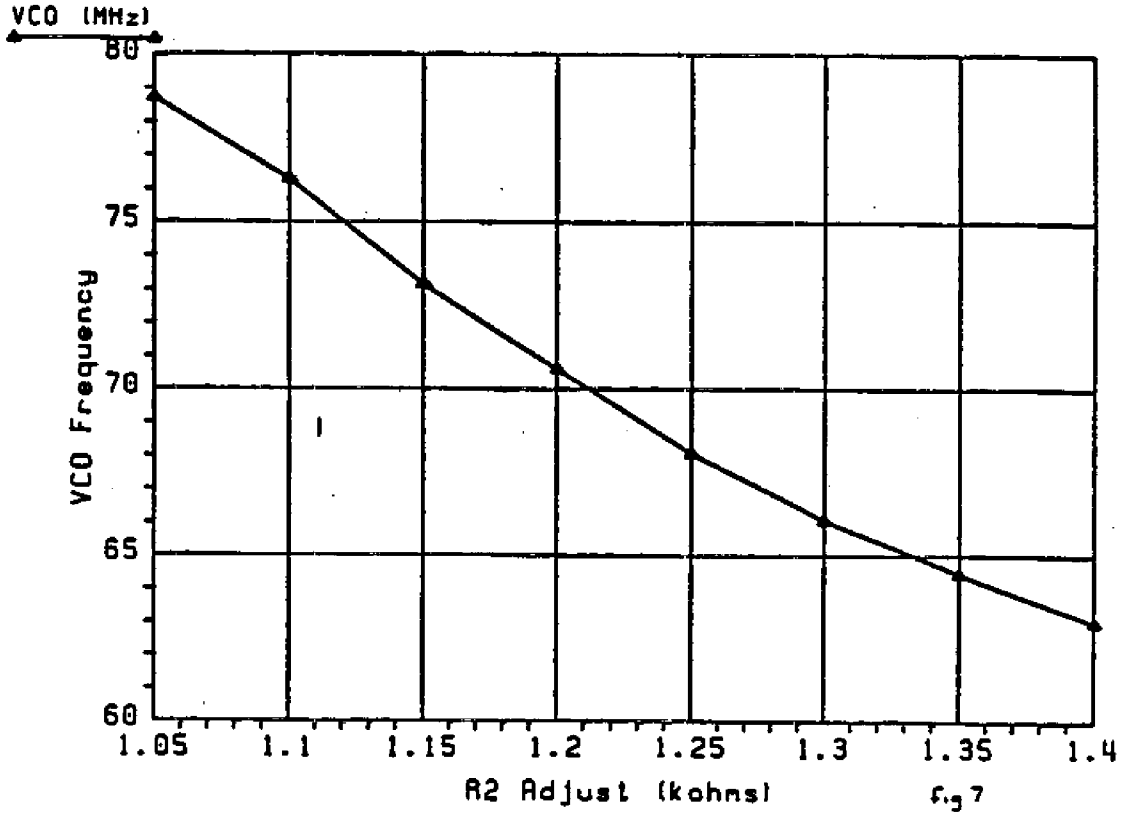

VCO (MHz)
VCO Frequency
60
65
70
75
80
1.05
1.1
1.15
1.2
1.25
1.3
1.35
1.4
R2 Adjust (kohms)

fig 7

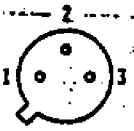
Appendix D

2N2369A NPN Bipolar Junction Transistor Specifications

CASE 22
(TO-18)

NPN silicon epitaxial transistor for high-speed range of 10 – 100 mAdc switching applications. Specifications provided at -55°C to +125°C for critical dc characteristics.

Collector connected to case



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.5	Vdc
Collector Current — Continuous	I_C	200	mAdc
Peak (10 μs Pulse)		500	
Total Device Dissipation @ T_A = 25°C	P_D	0.36	Watt
Derate above 25°C		2.06	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	1.2	Watts
Derate above 25°C		6.85	mW/°C
Operating Junction Temperature Range	T_J	+200	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Indicates JEDEC Registered Data

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 1 — t_{on} CIRCUIT — 10 mA

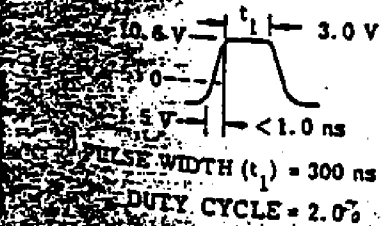
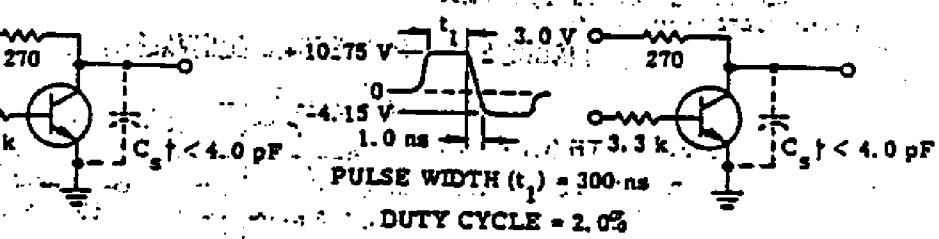


FIGURE 2 — t_{off} CIRCUIT — 10 mA



† Total shunt capacitance of test jig and connectors.

2N2369A (continued)

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 10 mAdc, I_B = 0)	-	BV_{CEO}	15	-	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 µAdc, I_B = 0)	-	BV_{CES}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µAdc, I_E = 0)	-	BV_{CBO}	40	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 µAdc, I_C = 0)	-	BV_{EBO}	4.5	-	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, V_{BE} = 0)	-	I_{CES}	-	0.4	µAdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0, T_A = 150°C)	-	I_{CBO}	-	30	µAdc
Base Current (V_{CE} = 20 Vdc, V_{BE} = 0)	-	I_B	-	0.4	µAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	-	h_{FE}	-	120	-
(I_C = 10 mAdc, V_{CE} = 0.35 Vdc)			40	-	
(I_C = 10 mAdc, V_{CE} = 0.35 Vdc, T_A = -55°C)			20	-	
(I_C = 30 mAdc, V_{CE} = 0.4 Vdc)			30	-	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			20	-	
Collector-Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc)	-	$V_{CE(sat)}$	-	0.20	Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = +125°C)			-	0.30	
(I_C = 30 mAdc, I_B = 3.0 mAdc)			-	0.25	
(I_C = 100 mAdc, I_B = 10 mAdc)			-	0.50	
Base-Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc)	-	$V_{BE(sat)}$	0.70	0.85	Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = +125°C)			0.59	-	
(I_C = 10 mAdc, I_B = 1.0 mAdc, T_A = -55°C)			-	1.02	
(I_C = 30 mAdc, I_B = 3.0 mAdc)			-	1.15	
(I_C = 100 mAdc, I_B = 10 mAdc)			-	1.60	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 100 MHz)	-	f_T	500	-	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 140 kHz)	-	C_{ob}	-	4.0	pF
Turn-On Time (V_{CC} = 3.0 V, $V_{BE(off)}$ = 1.5 V, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc)	1	t_{on}	-	12	ns
Turn-Off Time (V_{CC} = 3.0 V, I_C = 10 mAdc, I_{B1} = 3.0 mAdc, I_{B2} = 1.5 mAdc)	2	t_{off}	-	18	ns
Storage Time (I_C = 10 mAdc, I_{B1} = I_{B2} = 10 mAdc)	3	t_s	-	13	ns

(1) Pulse Test: PW = 300 µs, Duty Cycle = 2.0%

* Indicates JEDEC Registered Data

FIGURE 3 — STORAGE TIME EQUIVALENT TEST CIRCUIT