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FOCUS

Fiber Optic Camera Underwater System

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PROJECT FOCUS

INTRODUCTION

The Woods Hole Oceanographic Institution in Woods Hole, Massachusetts, is currently operating an Advanced Manuverable Underwater Viewing System (AMUVS) which delivers real-time video from underwater areas that are difficult to observe by other viewing techniques. Deployed and controlled from a manned submarine, the AMUVS and its tether system utilize manuverability and small size for observation of submerged objects and confined areas. The AMUVS is controlled by the manned vehicle ALVIN, and can operate at a maximum depth of 6000 meters.

A launch and retrieval system is designed to allow an operator in the manned sub to release the AMUVS and control both the vehicle movement and the umbilical cable deployment (Figure 1). As the operator manuvers the vehicle remotely, a black and white video camera mounted in a titanium pressure housing relays views of the surroundings to the manned submarine.

Having successfully demonstrated the AMUVS - ALVIN system, the Deep Submergence Laboratory (DSL) of WHOI proposed improvements and alterations in the existing design. DSL desired to have the real-time, black and white video display replaced with a color signal. The umbilical cable of the AMUVS, however, creates several problems prohibiting the direct installation of such a system. The video signal, as well as other control data and power, are sent across the metal conductors in the cable.

FIG. I – GENERAL ARRANGEMENT

VIDEO CAMERA
-REAL TIME

F/O CABLE

BOTTOM VIEWPORT

AMUVS-II

ALVIN
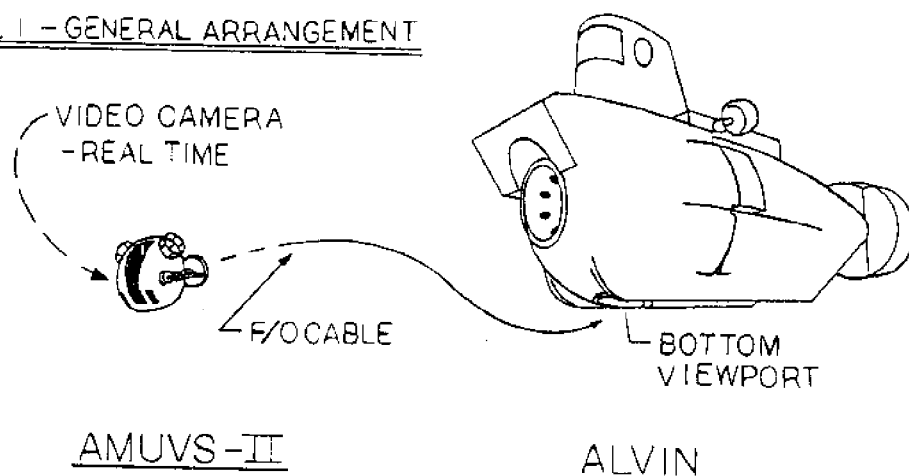
Figure 1: General Arrangement[2]

These conductors have a maximum data rate capability, which the current system is near approaching. By adding the color signal (which has a substantial data rate increase over black and white), the cable would have to be redesigned to accommodate the added bandwidth.

The cable is also a very restrictive element of the tether system: the length and mass of a metal conductor cable can be extremely difficult to manage, since twisting and tensile forces must be accounted for. The shear weight of such a cable itself is a problem, adding stress to the launch and retrieval unit and increasing the chances of a fouled tether.

The proposed solution that has been offered by DSL to support the color camera signal is to redesign the umbilical cable as a fiber-optic system.

The optical waveguide is capable of carrying substantially

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more data with less loss than a coaxial or paired-wire cable.
Figure 2 shows the attenuation versus frequency for three
transmission media. The loss in the optical fiber is virtually
constant, but the loss in the metallic transmission lines
increases with increasing transmission rates, thus creating an
upper limit of their use at high bit rates that is far below such
a limit for an optical waveguide (see Table 1).

Figure 2: Attenuation Versus Frequency[3]

Optical fibers also lack other troublesome properties
associated with metallic transmission media: they are
nonconductive, nonradiative, and noninductive. Ground loops and
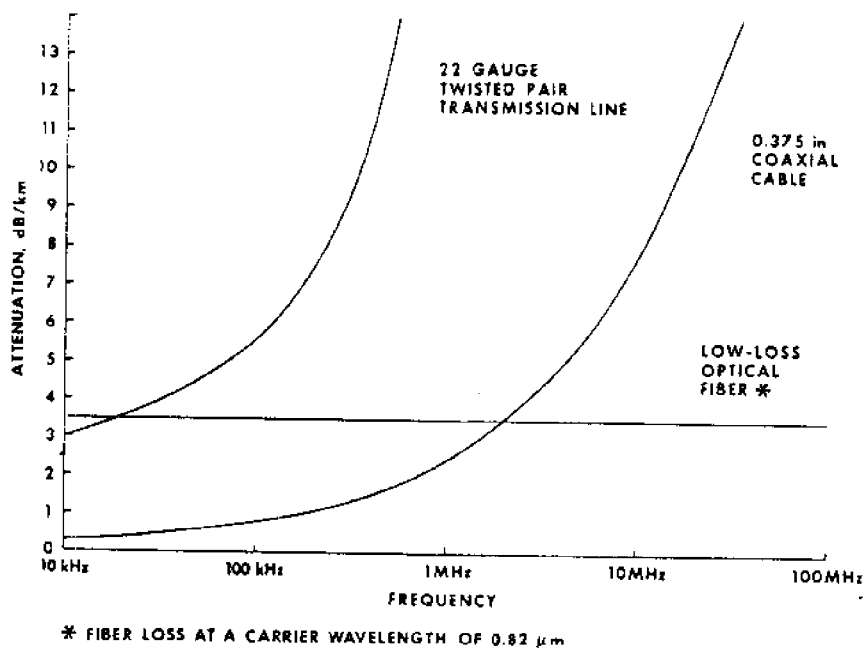radiative interferences that accompany coaxial cables do not
cause similar setbacks in optical systems.[5]

GROWTH CAPABILITY
TRANSMISSION MEDIA COMPARISONS

Transmission Media	Loss in dB/km at Half Bit Rate Frequency (Digital Transmission Rates)		
	T1 (1.544 Mb/s)	T2 (6.312 Mb/s)	T3 (44.736 Mb/s)
26-GAUGE TWISTED WIRE PAIR	24	48	128
19-GAUGE TWISTED WIRE PAIR	10.8	21	56
0.375-in-DIAMETER COAXIAL CABLE	2.1	4.5	11
LOW-LOSS OPTICAL FIBER *	3.5	3.5	3.5

* FIBER LOSS AT A CARRIER WAVELENGTH OF 0.82 μm

Table 1: Growth Capability[4]

The small size and light weight of optical fibers are also advantageous, since less stress will be put on the launch and retrieval unit, and deployment of the cable will be substantially easier. Optical fibers also have a small minimum bending radius, adding to easier tether management.

Also very important in the redesign of the AMUvS umbilical cable is the flexibility of system growth. As mentioned previously, bit rates are restricted in metallic conductors. The optical fiber not only allows for the added color camera bit rate, but also allows for further growth should any more high-bit capacity instruments or controls be introduced to the AMUVS. Current plans of DSL include the addition of yet another color camera to provide stereo viewing. Also in the makings are thoughts of building a small manipulator arm that would be controlled remotely. The optical system would allow for these expansions and restrict the necessity for design alterations to the electronics at either end.

THE FOCUS DESIGN

The department of Ocean Engineering at the University of New Hampshire offered Woods Hole a team of engineering students to design, construct, and test an optical system for the ALVIN/AMUVS. The result was project FOCUS (Fiber Optic Camera Underwater System).

In terms of general operation, the FOCUS system needed to be low-cost, with ample protection and durability in order to function in normal underwater missions. The optical link also demanded facile maintainence and service, both on the surface ship and in drydock.

Penetration of the ALVIN's pressure housing also introduced a formidable design constraint. Because the submersible is a manned vehicle operating at extreme ocean depths, any hull penetration needs to undergo rigorous safety testing by the United States Navy. These test procedures are tedious, expensive, as well as time consuming (on the order of two to three years), but nonetheless necessary to insure the well being of the operators and passengers. Since the ALVIN's only existing penetrators are electrical penetrators, FOCUS proposed using an optical path through the ventral Plexiglas viewport (the one least used by the pilot in navigation). While by-passing the safety hazards just mentioned, this technique also created the need for a sturdy and practical support mechanism for the optical equipment both inside and outside the submersible. Figure 3 shows the basic optical system.

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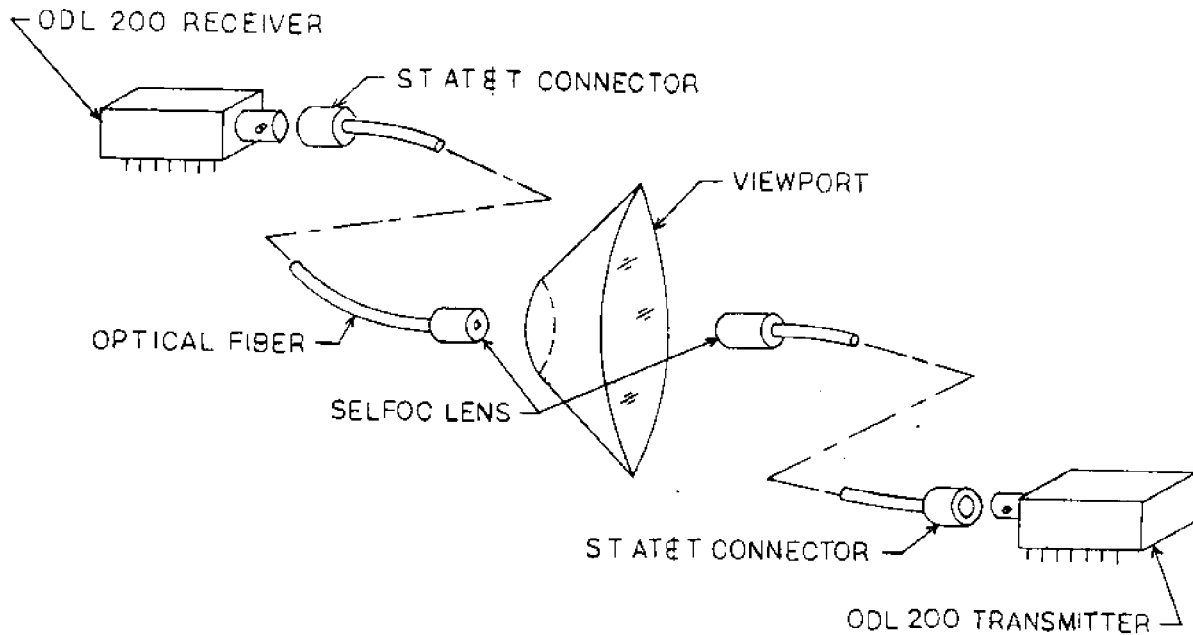
Figure 3: Optical System[6]

THE OPTICAL DESIGN

THE FIBER

Woods Hole provided Focus with the following characteristics of the fiber that will be used in the design:

- Multimode, with a graded index

- Bandwidth of 650 MHz * km

- Core diameter: 50 microns

- Cladding diameter: 125 microns

- Losses:

    <= 3.5 dB/km at a wavelength or 850 nm

    <= 1.0 dB/km at a wavelength of 1300 nm

- Numerical Aperture (NA): 0.2

(See Appendix A for discussion of these terms)

OPTICAL TRANSMISSION AND DETECTION

The optical transmitter/receiver package that FOCUS is using is the AT&T ODL 200 Lightwave Data Link, a pair of chips that satisfies the signal requirements.

Most importantly, the ODL 200 is designed for data rates that range from 40 to 220 Mb/s, thereby providing sufficient speed to handle the 160 Mb/s converted camera signal. Some of the other characteristics of the ODL pair that apply to the FOCUS design are:

- An integral lens-coupled optical connector that is compatible with AT&T's ST ferrule lightguide cable connector. Using these connectors on our optical cable, the fiber can readily be attached to the transmitter and receiver.

- A long wavelength (1300-1350nm) that falls in the range of maximum efficiency calculated for the system fiber.

- An operating temperature of 0 to 70 degrees C, and a storage temperature of -40 degrees C.

- A typical optical power of -15.5 dBm.

- A Pulse Width Distortion(PWD) of 0.5 ns

- Spectral Width of 170 nm.[7]

It should be noted, however, that the test system

constructed at UNH uses an ODL pair that is compatible with fiber having a 62.5 micron core and a 125 micron cladding. Due to time constraints and limited funding, this transmitter/receiver pair was more readily available and less expensive than the pair designed for 50/125 micron fiber. The optical and communications principles being virtually the same in both systems, FOCUS used the 62.5/125 system for proof of concept. A diagram of the optical portion of the system is shown in Figure 4.

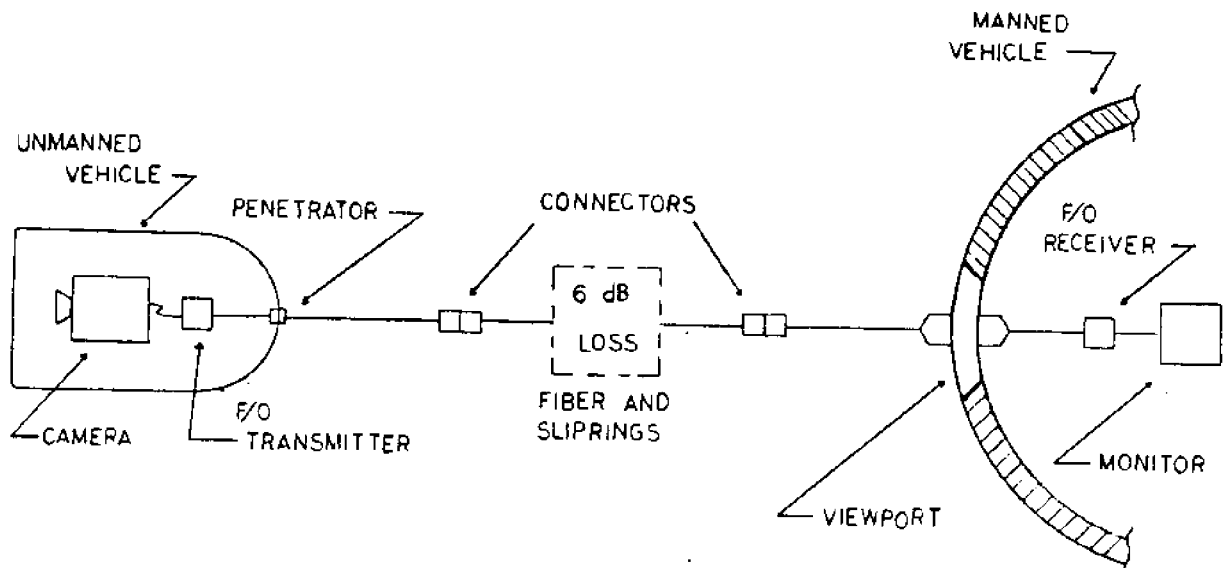Figure 4: Optical Link

The transmitter is driven by the communications electronics (dicussed later) and couples the optical signal into the fiber by means of the AT&T ST connector. The data propagates down the fiber and is delivered to a specialized lens, which aids in the delivery of the light to the viewport face. The signal is picked up on the other side by a similar lens, and continues along the

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fiber where another ST connector attaches it to the receiver, completing the optical link. The complete transmitter and receiver characteristics are summarized in Appendix E.

The crux of the optical design is the transmission of the optical pulses through the viewport of the ALVIN (Fig. 4). The design of such a system involved cautious and careful analysis of several optical principles, some of which are discussed here to justify the FOCUS prototype.

Surface refraction is the bending of light as it travels from one transmission medium to another. The change in direction is due to the materials having different indices of refraction (the refractive index is simply the ratio of the speed of light in a vacuum to the speed of the light in the medium). Snell's law describes the refraction concept, and is illustrated in Figure 5.

$$n_1 \sin \Theta_1 = n_2 \sin \Theta_2 ,$$

where

n_1 = refractive index of incident medium,

n_2 = refractive index of refraction medium,

Θ_1 = angle of incidence,

Θ_2 = angle of refraction.

A wave moving from a lower index of refraction to a higher index has an angle of incidence greater than its angle of refraction. Likewise, a signal traveling from a larger to a smaller refractive index will have an angle of refraction that is greater than its angle of incidence. Figure 5 also shows a

reflected beam (dotted line). These reflections are called
Fresnel reflections and involve a power loss due to a difference
of refractive indices. Two materials that have the same indices

INCIDENCE

REFLECTION

θ_1 θ_1

n_1

n_2

TRANSMISSION

θ_2
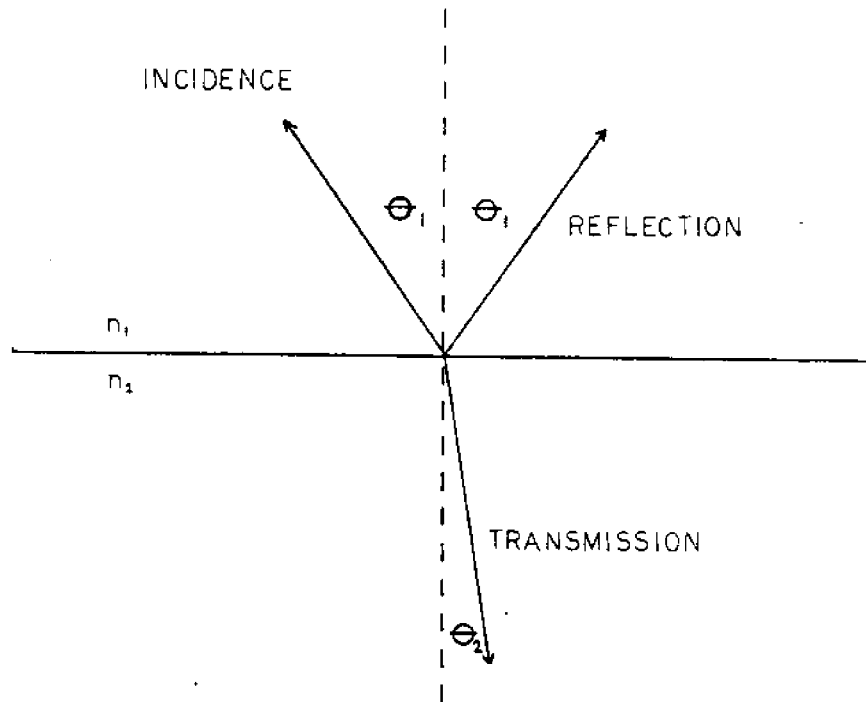
Figure 5: Snell's Law and Index of Refraction[8]

of refraction mathematically have no reflections, and
consequently zero power loss due to reflections.[9]

Figure 5 shows that the angle of incidence and the angle of
reflection are equal, but in general these are not equal to the
angle of refraction. The refracted beam is in line with the
incident beam when the angle of incidence is zero. This requires
that the light be introduced perpendicular to the viewport face.
Reflections still exist, however, because the light signal has to
travel across the air gap between the fiber and the glass face.
To minimize these losses, index matching fluid is needed to

"smooth" the barrier crossing and prevent the optical signal from bending. In the FOCUS system, the glass fiber index and the index of the Plexiglas viewport were not the same, so a fluid was used that represented the average of the two boundary indices. While reflection losses were not totally eliminated, they were reduced substantially from those that occurred when the light crossed through air to get to the viewport. Table 2 shows the refractive indices of the optical components.

$$n_v = 1.570, \text{ viewport (determined experimentally; see Appendix B)},$$

$$n_{fl} = 1.515, \text{ Index Matching Fluid.}$$

Table 2: System Indices of Refraction

Other important properties in optical analysis are diffraction and numerical aperture (NA). Diffraction results in random change of direction of the light, due to imperfections or obstructions in the surface and volume of the viewport, and the result is a loss in optical power.

Light data from an optical transmitter is composed of many rays of light traveling down the fiber at different velocities. The numerical aperture of a fiber explains the angle at which the light travels, and is defined as

$$NA = \sin \Theta_i ,$$

where Θ_i = the angle of acceptance.[10] (Figure 6)
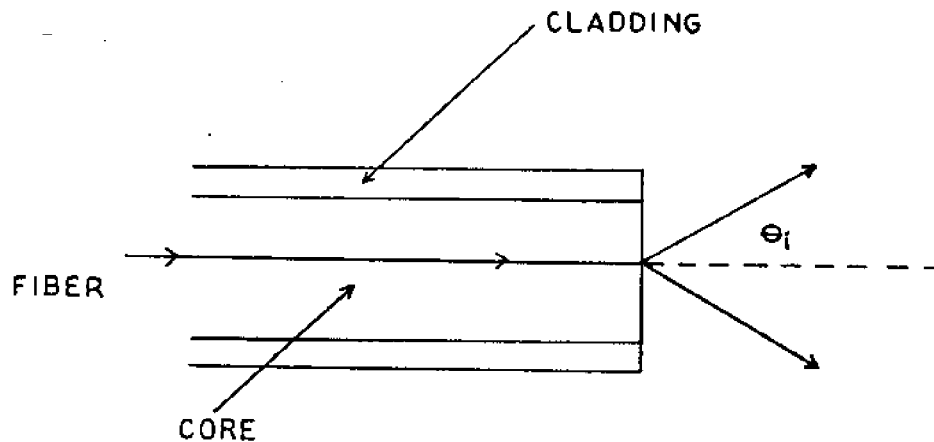
Figure 6: Numerical Aperture of a Fiber

The fiber has a cladding which keeps the light in its core.
(see Appendix A).   This cladding is a glass of a lower index of
refraction than that of the core index, thereby forcing the light
to strike this cladding in a certain range of angles. The light
is then reflected back into the fiber core, and there is no loss
of light.   The viewport, however, does not have this
core/cladding interface; instead, it has a uniform refractive
index throughout.   Therefore, without special attention, the
signal will not travel through the viewport as a concentrated
beam and will be difficult to recover.

The problems of numerical aperture and diffraction can be
solved by transmitting a collimated beam of light through the
viewport.   A collimated signal provides a wide beam so that the
chances of losing the entire signal (due to diffraction) are
greatly reduced.   A collimated beam also aligns all the light
rays so that they are incident normal to the viewport face,

forcing the light to travel straight through the Plexiglas.

Collimated beams are most easily achieved by using a device called a SELFOC lens (SELf FOCusing; Patent under NSG America, Inc.). A SELFOC lens is a glass rod with an index of refraction that decreases from its axis to its periphery along the radius (see Appendix C). This varied refractive index causes a light ray traveling outwards from the axis to be bent back towards the center of the lens, as shown in Figure 7.[11]
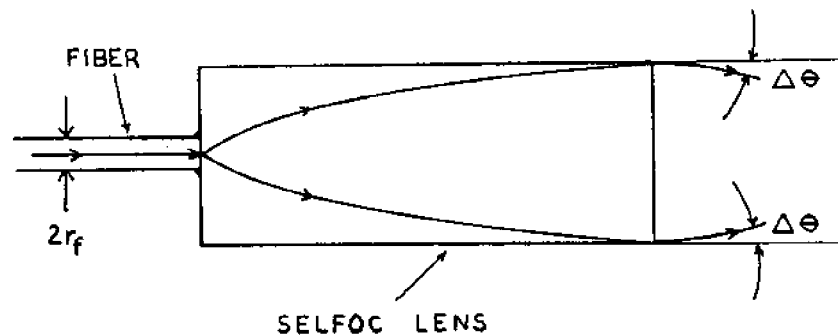
Figure 7: Geometry of Light Rays in a SELFOC Lens[12]

It is desired to have $\Delta \Theta$ in order to obtain perfect collimation. is given by

$$\Delta \Theta = n_o \sqrt{A} \, r_f \, ,$$

where n_o = refractive index of axis of SELFOC lens,

$\sqrt{A}$ = quadratic gradient constant of the lens, and

r_f = diameter of the fiber.

As a rule of thumb, $\Delta \Theta$ is decreased when

$$n_o \sqrt{A} \, r_o >= \text{(NA) of the fiber}$$

when the working distance from the target is zero , r_o is the radius of the SELFOC lens, and

NA of the lens $\cong$ NA of the fiber.[13]

There are two SELFOC lenses in the FOCUS design. The first is placed on the outside of the viewport, and functions to collimate the beam. The second is used on the other side of the viewport, inside the submarine. It recieves the collimated beam and directs it back into the fiber. It is important that the two lenses are aligned properly, or else the focused spot in the receiving lens will not align properly with the fiber. A typical alignment error is illustrated in Figure 8.
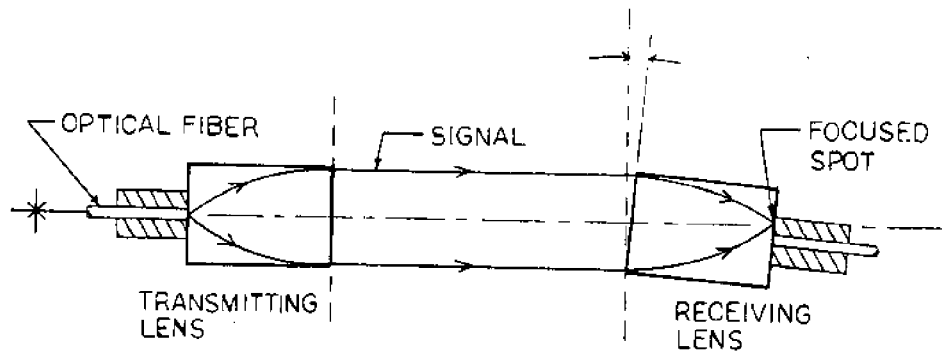
Figure 8: Misalignment of SELFOC Lenses[14]

The best lens for the FOCUS system was found to be NSG's SLS-1.0 (Appendix C). This particular lens, however, could not be obtained in time for the project deadline. Therefore, a SLW-1.8 (from NSG) lens was used instead, and was suitable for proof of concept.

The viewport/lens arrangement is shown in Figure 9. It

EXTERIOR
INTERIOR

SELFOC LENS
SELFOC LENS

SIGNAL

MOUNTING
ASSEMBLY

INDEX
MATCHING
FLUID

LIGHT BLOCK
VIEWPORT
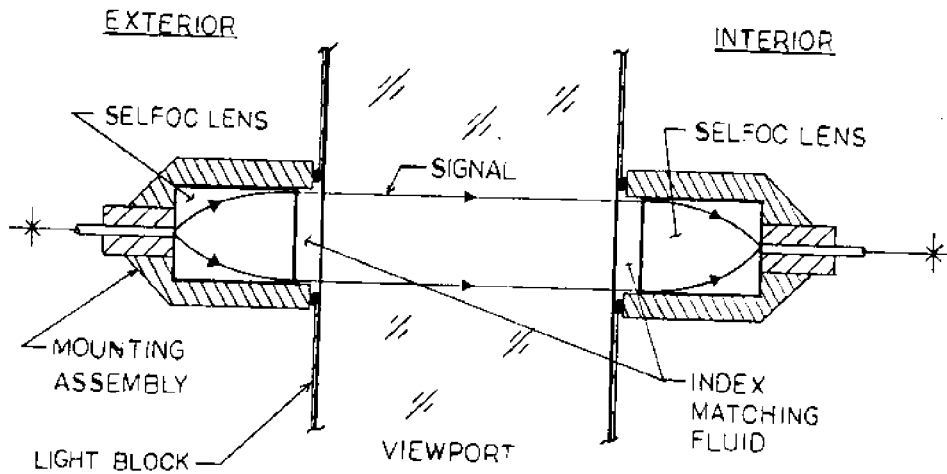
Figure 9: Viewport and SELFOC Lens Arrangement

describes the position of the SELFOC lenses relative to the
fibers, the index matching fluid, and the viewport. Figure 9
also illustrates a device called a light block. A light block is
important in keeping external light from entering the viewport
and interfering with the transmission signal.

MOUNTING APPARATUS AND POSITIONING

The performance of the optical signal as it penetrates the
viewport relies upon a suitable mounting scheme wnich allows for
positioning (aligning), durability, and consistent placement of

the connector assembly on both sides of the viewport. There are numerous design constraints which must be met to assure optimum operation.

The operating environment to which the system is exposed varies from a highly corrosive, high pressure one with wide temperature variations (i.e., the outside of the submersible), to one of a life-supporting environment existing within the ALVIN. Clearly, the major constraints occur with the exterior part of the mounting system. The ocean environment dictates that the mounting system be able to withstand hydrostatic pressures of up to 10,000 psi, be non-corrosive, and function over a temperature range of 0 to 100 degrees celcius.

The effects of hydrostatic pressure on the system is of primary importance. The preferred high pressure connector, manufactured by Giannini Petro-Marine, employs the use of a SELFOC lens assembly[15](Figure 10). The positioning of the male/female "halves" of the connector against the viewport creates voids or chambers which must contain index matching fluid.

On the exterior side of the viewport, the high pressures incurred will have an adverse effect on the fluid chamber due to the large pressure differential between the chamber and the exterior hydrostatic pressure. The system must therefore be designed to minimize the pressure differential by means of a pressure compensation device. The SELFOC lens contained in the high pressure connector has been designed and tested to withstand pressure up to 10,000 psi, the fluid chamber pressure at maximum operating depth. This pressure compensation device (Figure 11)

Figure 10: Giannini Connector & Penetrator

ROV OPTICAL ARRANGEMENT

REMOVABLE CONNECTION

SELFOC LENS

GIANNINI UFO CONNECTOR

OPTICAL FIBER

PROPRIETARY SEAL

OPTICAL FIBER

SST MIDLOCK FERRULE

CONAX FMK PENETRATOR
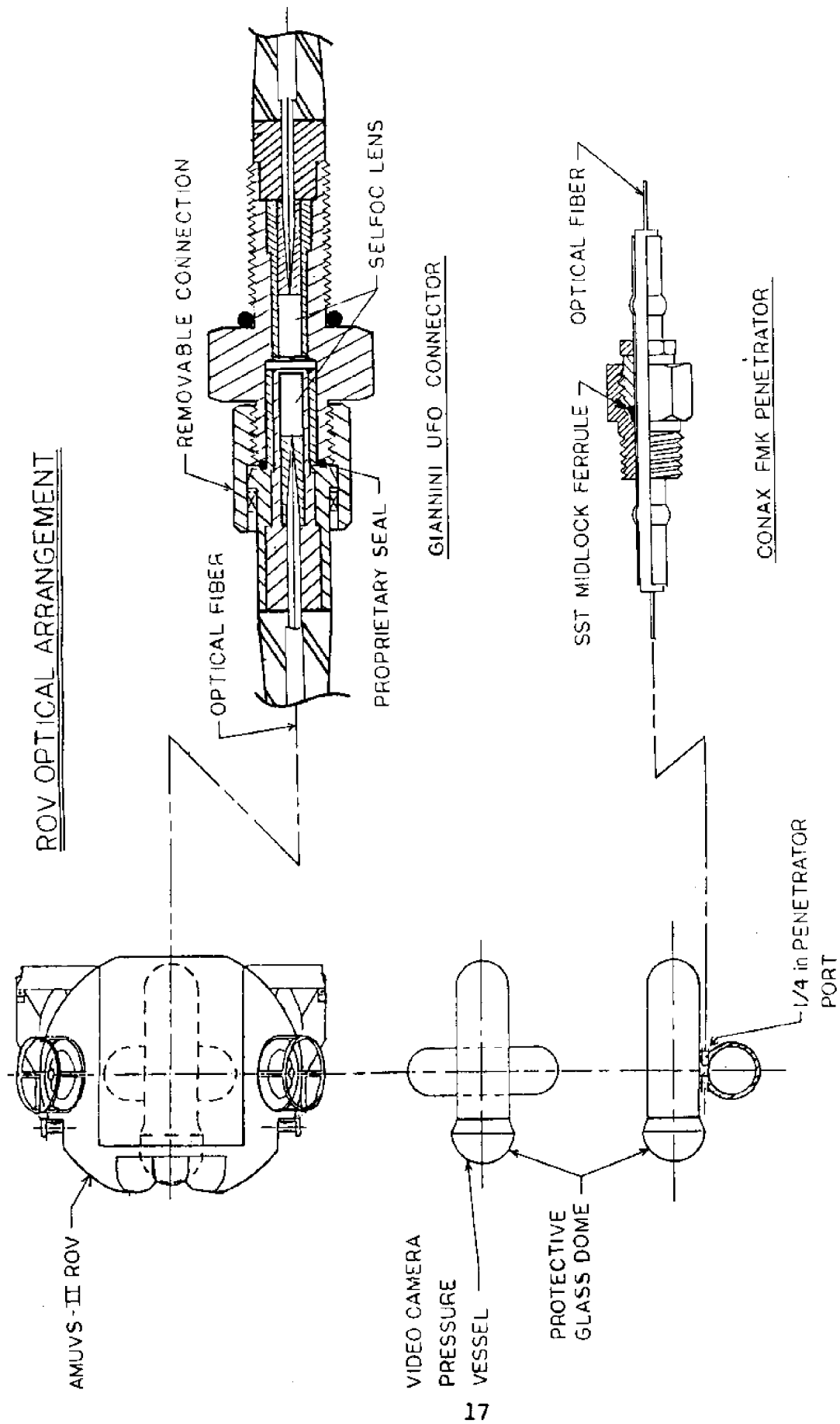
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AMUVS-II ROV

VIDEO CAMERA
PRESSURE
VESSEL

PROTECTIVE
GLASS DOME

1/4 in PENETRATOR
PORT

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Figure 11: Pressure Compensation Device
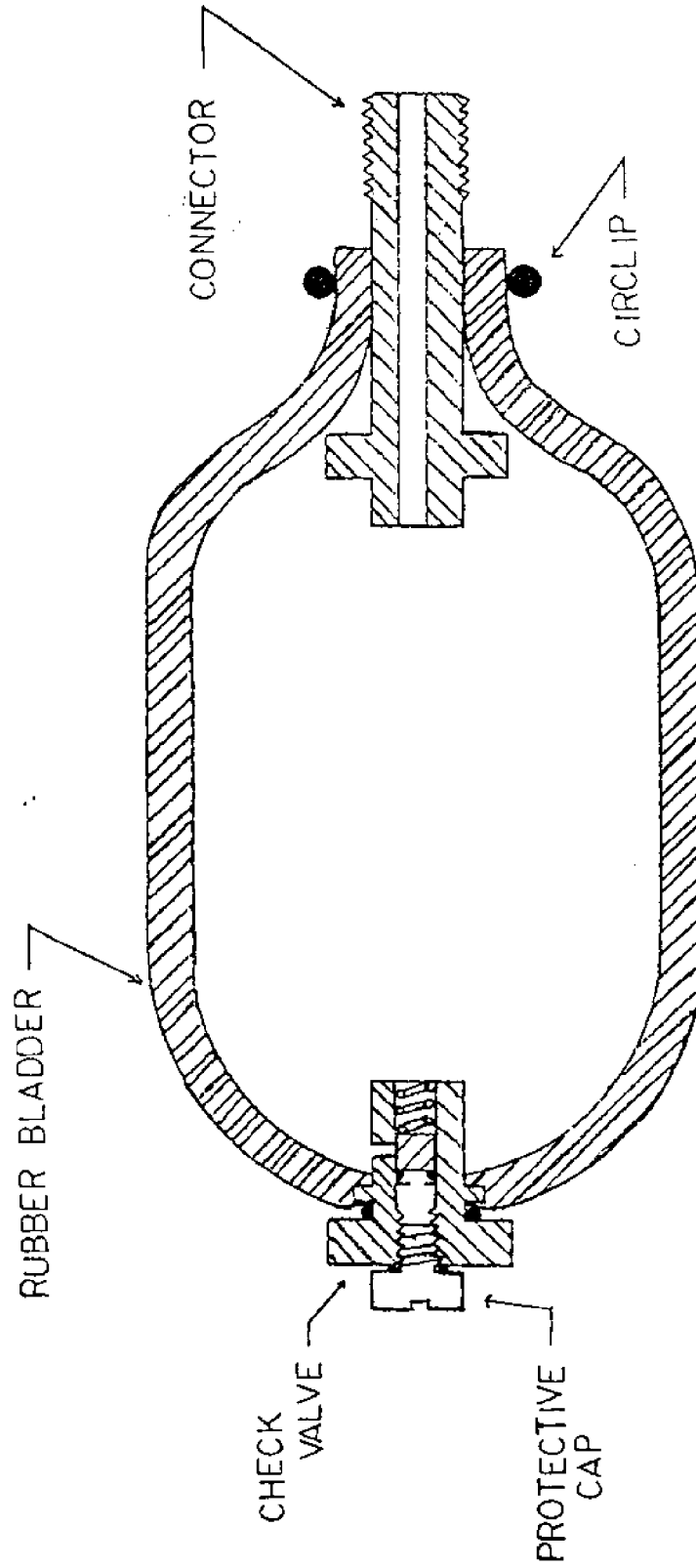
PRESSURE COMPENSATION SYSTEM

CONNECTOR

CIRCLIP

RUBBER BLADDER

CHECK VALVE

PROTECTIVE CAP

EXT-2

EXTERNAL MOUNTING ARRANGEMENT

VIEWPORT

COVER PLATE

CONNECTOR BUSHING

SELFOC LENS

BUNA-N O-RING SEAL

GIANNINI UFO CONNECTOR

OPTICAL FIBER

SEE DRAWING NO. EXT-3

SEE DRAWING NO. EXT-2

RETAINING COLLAR
- SEE DRAWING NO EXT-3

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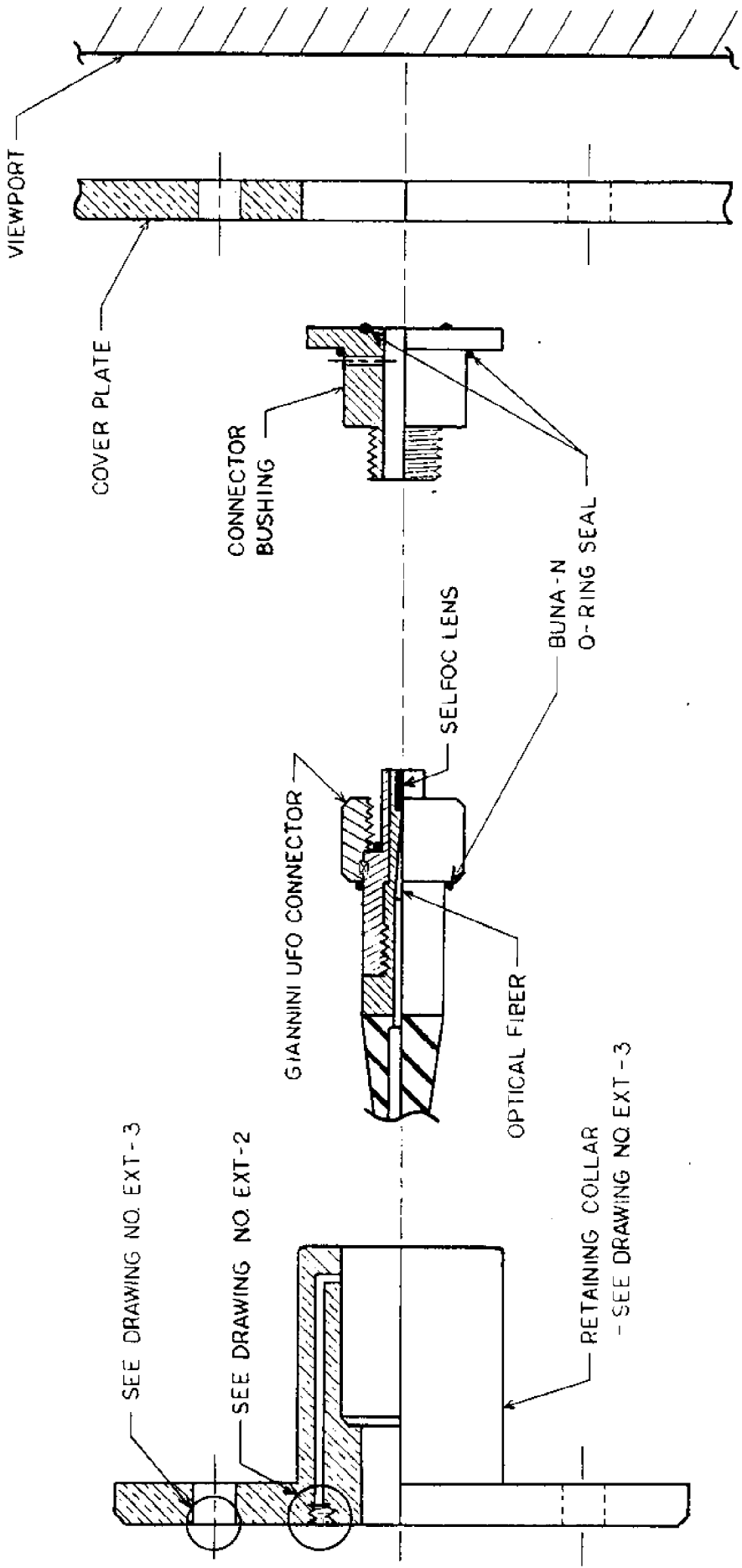
Figure 12:

External System

EXT-1

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is essentially a flexible rubber bladder fitted at one end with a coupler (to secure to the mounting assembly). The free end of the bladder is fitted with a one-way check valve to allow for filling and purging of the pressure compensation system. Index matching fluid is introduced by means of a syringe, which, when inserted into the check valve, will force the fluid into the chamber and out the fluid ducts. The objective of this design is to purge the air out of all volumes containing the index matching fluid. The system is filled and inspected to insure that no air is contained within, then attached to the protective cover plate (Figure 12), sealing the connector against the viewport. At this point, the syringe is removed and the check valve is capped to protect it from contaminants that may enter the pressure compensation device. This configuration allows for the small amount of compression and expansion of the adjacent metals as pressure changes. The considerations of size, ease of assembly, and maintenance have been incorporated into the design of the pressure compensation system.

The characteristics of the index matching fluid must include only the desired refractive index, but it must also be stable at high pressures and over large temperature variations. In addition, the fluid must possess suitable viscosity at all times during operation.

The pressure compensation device is attached to the face of the retaining collar (Figure 12) which contains the high pressure connector. The purpose of the retaining collar is to center the connector and force the connector bushing against the viewport to

create the index matching fluid chamber. The collar is composed of two halves which are fastened together around the fiber optic cable, thereby avoiding the need to manufacture the collar onto the cable as the connector is being attached.

Due to the high compressive pressures the viewport sustains, inward movement of up to 1/8 of an inch. A mounting system must be designed which allows for this movement and maintains the connector's water-tight seal against the viewport. To accomplish this function, the retaining collar, which secures the connector assembly against the viewport, was designed to move with the viewport. The mechanism allowing for the inward-outward motion (Figure13) is achieved by sliding the retaining collar over four studs affixed to the cover plate. Compressive springs are then secured against the retaining collar by means of locking nuts. The locking nuts are positioned on the studs to develop the necessary compressive force on the retaining collar to keep it against the viewport. Binding between the retaining collar and the studs is allieviated by a bushing between the two surfaces. The springs are enclosed by a protective cover which prohibits foreign particles from becoming lodged between the coils.

As was previously mentioned, the materials used in the mounting assembly are exposed to the corrosive sea-water environment. This dictates the use of titanium metal parts and rubber parts which retain their integrity throughout operation. Titanium is the primary metal used for components exposed to sea water due to its excellent corrosion resistance. Additional beneficial properties include: a relatively low density, good

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RETAINING COLLAR

COMPRESSIVE MOUNT ARRANGEMENT
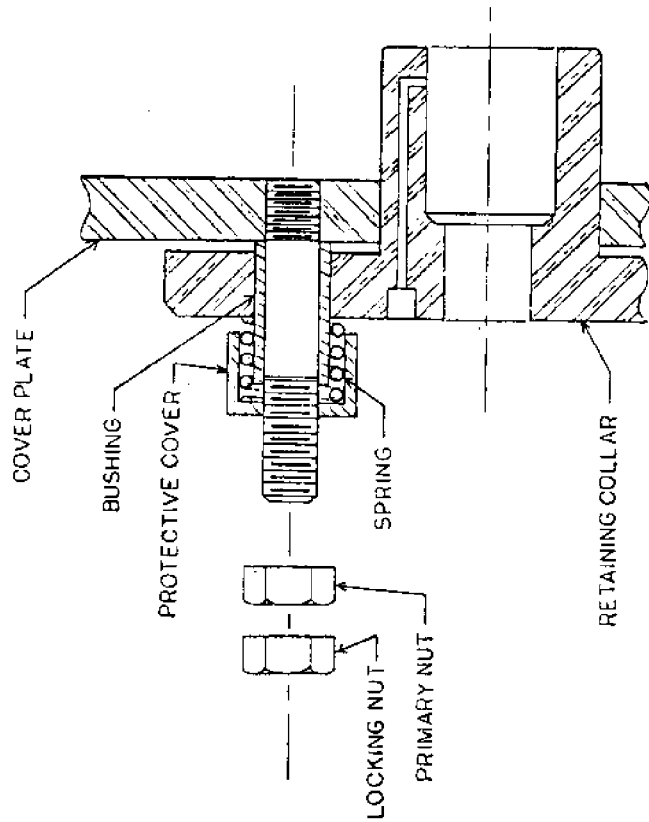
PARTING LINE - 2 SECTIONS

THREADED HOLE (2)

MOUNTING HOLE (4)

FLUID DUCT

RECESS BORE (2)

COVER PLATE

BUSHING

PROTECTIVE COVER

SPRING

RETAINING COLLAR

LOCKING NUT

PRIMARY NUT
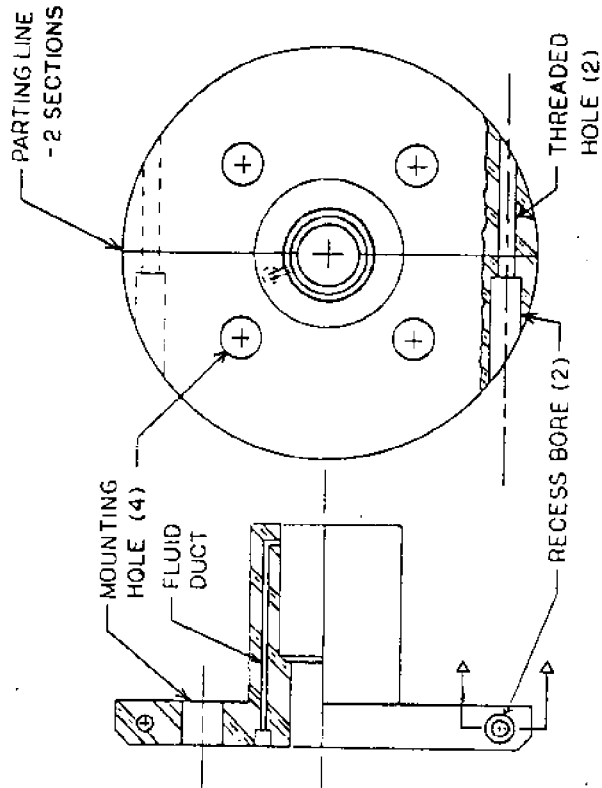
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N.T.S   14 MAY 1986

EXT-3

Figure 13: Shrinkage Compensation System

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strength, easy fabrication, and the ability to withstand temperature extremes.

The exterior mounting assembly requires a durable design and minimal protusion from the viewport. Although the ALVIN is protected by a cage, there may be instances of objects passing through this cage and impacting on the mounting assembly. To reduce the possibility of such interference, the overall height of the system was designed to be kept to a maximum of 8.7 cm. This dimension is based on the distance that adjacent electrical penetrators extend out from the hull. The cable will exhibit negligible stress on the mounting assembly, as it is fastened to the syntactic foam surrounding the hull. However, the possibility of the cable becoming snagged is recognized and incorporated in the design.

Coupled with the aforementioned physical design constraints, the system is designed to keep installation, maintenance, and service procedures as brief and as inexpensive as possible. Installation experience and tools are kept to a minimum, and replacement of components can be accomplished efficiently.

The interior mounting of the female half of the high pressure connector experiences many of the same constraints as the exterior assembly, with the exception of the pressure compensation system. The interior assembly must move with the viewport while maintaining a seal against the viewport. To accomplish this, a 1.0 inch thick plate, fitted with a large 2.0 inch diameter O-ring is inserted into the recessed area adjacent to the viewport (Figure 14). The plate is designed to mate with

the geometry of the recessed area and rest on the O-ring, creating a seal. The O-ring dimensions are such as to allow for the compression due to the movement of the viewport while the plate is held stationary.

As with the exterior connector, a chamber is necessary to contain the index matching fluid between the SELFOC lens and the viewport. This reservoir chamber is created by the O-ring seal against the viewport. Prior to inserting the connector into the plate, the reservoir is filled with fluid to insure that only index matching fluid exists between the SELFOC lens and the viewport. A gasket is adhered to the 1.0 in. plate to interface with the hull. The purpose of this gasket is to allow for shrinkage of the hull by alleviating the possibility of pinching or binding. The gasket is 1/16 in. thick and is made of closed-cell neoprene sponge. The O-ring used for the seal is made of Buna-N material and has 40 durometer specification. Neither material decomposes due to the index matching fluid, and both retain their integrity after cyclical loading is experienced.

An additional constraint requires that the interior mounting assembly cannot be permanently affixed to the pressure hull. Options for securing the connector assembly are very limited; it was concluded that a suitable means for securing the system was to use two existing studs (that are used to hold the submarine floor down). A mounting plate was constructed to utilize these studs, and allows for quick installation and removal of the mounting system (Figure 14).

The mounting plate not only holds the 1.0 in. plate in position, but is also fitted with a two-axis translational

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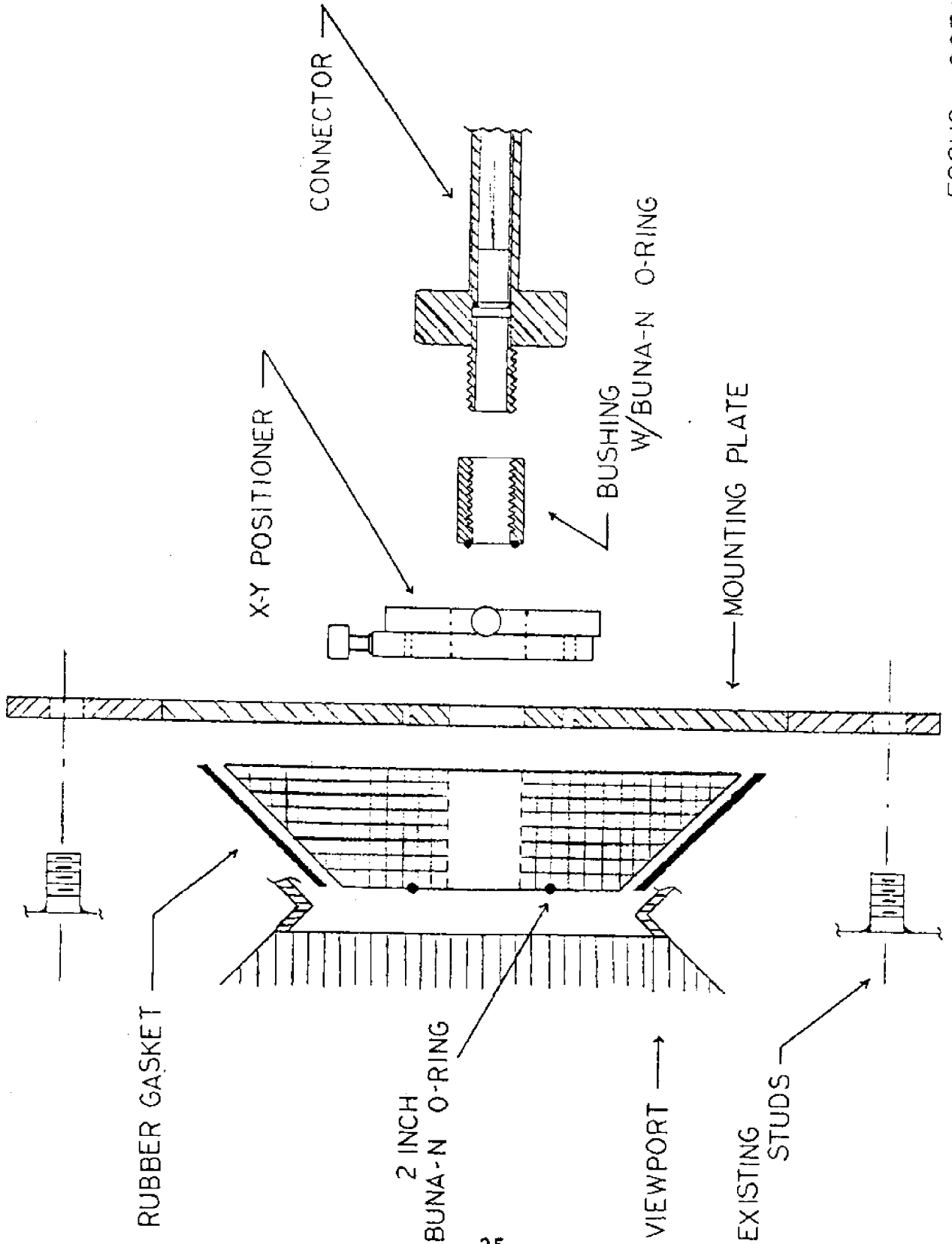
Figure 14: Internal Mounting Mechanism

INTERNAL MOUNTING ARRANGEMENT

CONNECTOR

X-Y POSITIONER

BUSHING W/BUNA-N O-RING

MOUNTING PLATE

RUBBER GASKET

2 INCH BUNA-N O-RING

VIEWPORT

EXISTING STUDS

positioner. This positioner, supplied by Ealing Electro-Optics, Inc., is necessary to adjust the position of the connector (and SELFOC lens) to align with the incoming optical signal. Additionally, the connector is secured by the positioner, maintaining the appropriate distance between the SELFOC lens and the viewport .

The overall height of the mounting system must be within the 3.375 in. existing between the hull and the subfloor; this is accomplished by the FOCUS design.

The material for the 1.0 in. plate and the mounting plate need not be titanium, but does need to be specified to avoid galvanic action and give the desired strength to secure the system in position. Again, ease of installation and service are objectives which are met with this design.

The AMUVS Remote Operation Vehicle (ROV) employs the use of the same high pressure connector being used for the viewport interface. The purpose of this connector is to allow for quick disconnection of the fiber optic cable from the ROV, rather than having the cable permanently fixed to the vessel. The connector will be utilized in a conventional manner, that is, it will not be separated by any distance. Provisions shall be made to secure the connector to the syntactic foam hull to eliminate stresses developed during operation.

The penetration of the fiber through the camera housing is accomplished by employing a Conax-Buffalo Corp. fiber optic bulkhead penetrator. The port existing on the housing requires the thread diameter of this penetrator to be 0.25 in., so a

standard FMK-A-50 model was specified. The purpose of this penetrator is to allow a continuous fiber to pass through the housing for uninterrupted operation. The Conax penetrator is tested to 15,000 psi and has an operating temperature range of -40 to 205 degrees C.

For laboratory testing of the entire electrical-optical-mechanical system (and also for demonstrating purposes), a model emulating the viewport arrangement was constructed. The viewport, on loan from WHOI, is mounted in a frame constructed to the specifications of the hull immediately surrounding the viewport. A model of the interior mounting assembly has also been constructed, with the exception of the Giannini high pressure connector. Components include the 1.0 in. plate, the mounting plate, and the positioner. Exterior modeling of the mounting system will not be developed until the proof-of-concept for the signal transmission is verified. For testing purposes, the high pressure connector is replaced by two SELFOC lens assemblies. The lenses will be positioned to allow for a chamber to be filled with index matching fluid. The exterior assembly will be secured by sliding the SELFOC lens holder through the protective cover plate, and retained by a collar fixed to the cover plate. The interior assembly follows the same format, except that the SELFOC lens holder is secured by a collar mounted on the positioner, which allows for aligning the lenses. This mounting system approximates the actual system without the major constraint of high pressure.

DIFFERENTIAL PULSE CODE MODULATION

There are many methods of transmitting analog information across a digital channel. The most common is known as pulse code modulation (PCM). PCM is essentially an analog message that is represented by a coded group of digital pulses. A variation of PCM is delta modulation (DM).

Delta modulation (DM) is the simplest method for converting an analog signal to digital form but also requires a larger transmission bandwidth than PCM. The theory behind DM is that the message is compared to a stepwise approximation by subtraction, the difference being passed through a hard limiter whose output equals +delta or -delta, depending on the polarity of the difference.[16] Since there are only two possible outputs of the limiter, the result is a binary waveform.

A step beyond delta modulation is differential pulse code modulation (DPCM). Once again, a difference signal between the message and a previously sampled portion of the message is created. With DPCM there is now a pulse coded representation of a differential signal as opposed to a binary step. This allows the system to better respond to large changes of amplitude in the input signal. The advantages over delta modulation are balanced by more complexity in the circuit--about the same as a PCM circuit.[7] When compared to PCM, DPCM has the advantage of using fewer bits to transmit the same amount of information. To illustrate this, nine bits are used with PCM to give acceptable color video-signal reproduction as opposed to three bits for

DPCM.[18]   The FOCUS design incorporates six bits of information in its transmission for a higher degree of resolution in the reconstructed color signal.

In summary, differential pulse code modulation was chosen for various reasons. Since only six bits of actual video information are being transmitted instead of nine bits, circuit complexity was reduced. It was also determined that it was less likely to lose information with fewer bits transmitted. A third reason is that since there are six bits of information, the possibility of replacing part of the transmitted code with additional timing information, control signals or another color camera could be considered more easily in future efforts.

Several factors were taken into consideration in the design of the FOCUS electronics: size, speed and the fact that information is to be sent across only a single fiber optic cable. Restricting transmission to a single fiber optic cable was a major design task for FOCUS. This required increasing the transmission speed by a factor of however many bits were being transmitted. In addition to increased speed, more complex parallel-to-serial conversion circuitry is required. The same is true for serial-to-parallel conversion at the receiver. The additional conversion and serial transmissions require very fast operations if a color video signal is to be accurately reproduced. A high speed logic family known as Emitter Coupled Logic (ECL) was chosen to implement the FOCUS design.

ECL offers several advantages over other logic families. These advantages include high switching rates, low propagation delays with moderate edge rates, and the ability to drive low

impedance transmission lines.[19] Temperature compensation is also available on most ECL components. Although ECL is extremely static sensitive and requires great care in handling, it has the performance characteristics that best suit the design requirements.

Although power consumption was not a major design constraint, power dissipation in the form of heat must be taken into consideration. This poses no significant problem for the receiver as that will be located on an equipment rack in the submersible ALVIN where adequate air flow can be obtained for cooling. Power dissipation in the transmitter circuit poses no problem in the desk-top model; adequate air flow is available here also. When the circuit is contained in the small titanium pressure hull of the AMUVS where there is no air flow at all, an alternate form of heat sink will have to be used. One proposed solution is to use the hull as part of the heat sink since it is approximately the same temperature as the surrounding environment (three degrees Celcius at operating depth).

Another consideration is the environment in which FOCUS will operate. The receiver, as stated earlier, will be in the ALVIN, an environment which most electronics are capable of handling. The transmitter, however, will be operating in temperatures ranging from about three to over forty degrees Celcius, and both will need to be operable in all weather conditions on the deck of the ship. For these reasons, chips of military specifications were used when available.

THE ELECTRICAL SYSTEM

TRANSMITTER

Introduction

The transmitter takes the raw video signal and converts it to a digital signal for optical transmission. The video signal is sampled using Differential Pulse Code Modulation (discussed in a later section). The digital sample is then sent serially across the optical fiber.

General Theory

The transmitter is designed to sample the video signal every 100 nanoseconds for a sampling frequency of 10 MHz. This is 2.4 times the highest frequency contained in a color video signal, thereby satisfying the Nyquist sampling criterion. Six bits of data, including an overflow bit are used to represent the amplitude of each sample. These six bits are then combined with a nine bit flag code for transmission. The purpose of the flag code is data and clock synchronization in the receiver.

Detail of the Transmitter

The following is a detailed discussion of the transmitter. It will be helpful to refer to the Transmitter Block Diagram Schematic and Timing Diagrams in Appendix F.

The video signal enters the circuit through a buffer. This buffer isolates the transmitter from the camera and provides the proper impedance match to the incoming line. The buffer is made

of a high frequency operational amplifier, with at least a 5 MHz bandwidth.

The buffered signal then goes to a summing junction, where the reconstructed video signal from the last sample is subtracted from the incoming video signal. The output of this summer is the difference between the incoming video and what the video was at the last sampling time. This difference is what is eventually transmitted to the receiver. The summer is made up of another high frequency operational amplifier.

The differential signal is converted to a six bit digital code by the analog to digital converter (A/D). An Analog Devices AD9000 flash converter was chosen for this application, due to its small size, ultra-fast conversion time (13 nanoseconds), and compatibility with ECL logic.

The digital output of the converter goes to two places. The first is a digital to analog converter (D/A). This ultra high-speed converter recreates the analog differential signal that was originally sent to the A/D converter. A buffer is between the outputs of the A/D converter and the inputs of the D/A converter to insure the digital data is present for conversion. The reconstructed differential signal is then integrated. This integrated signal is the sum of all the differential signals, and thus it is the reconstructed video signal. It is this signal that is subtracted from the incoming video to create the next differential signal.

The second place the data goes to is the parallel to serial converter; this converter is a pair of eight-bit shift registers. The registers parallel load the six bits of data plus the nine

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bit flag code, and then serially shift out all fifteen bits, one at a time. This sixteen part cycle (one load and fifteen shifts) must repeat every 100 nanoseconds. This results in a transmission rate of 160 million bits per second.

The shift registers are clocked by a 160 MHz oscillator. A very high speed crystal oscillator with ECL logic levels will be installed. Currently the clock is being driven by a variable frequency oscillator for test purposes. The clock also drives a "divide by 16" circuit. This 10 MHz signal tells the shift registers When to load (as opposed to shift), and tells the A/D converter when to start converting.

The serial output of the shift registers goes to the AT&T ODL 200 electrical to optical converter, which delivers the light signal to the fiber.

Detail of the Receiver

The receiver is basically just the opposite of the transmitter. The optical fiber connects to the AT&T ODL 200 optical to electrical receiver. The converted electrical output connects to the serial to parallel converter shift registers.

The flag code comes into play as the data is being shifted into the registers. The format of the transmitted data is shown in Figure 15.

The format is made up of the nine bit flag code, which is sent first; the six bits of data are sent next. The last bit is a "don't care" bit, which represents whatever appears at the transmitter output when its shift registers are loading in the

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next data word to be sent out.
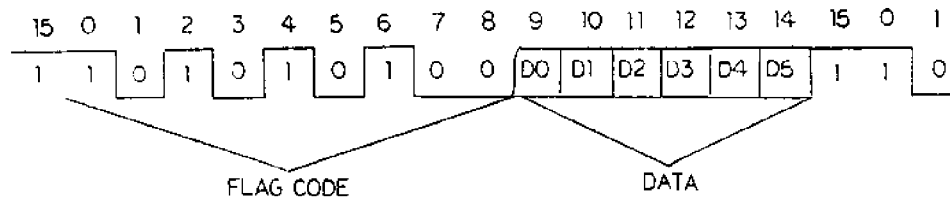
Figure 15: Transmitted Data Format

As the incoming flag code and data are shifted into the receiver shift registers, the flag code circuitry is checking to see if the zeros in the code are lined up. When the four zeros of the flag code line up, a signal is sent to the shift registers telling them to hold. A signal is also sent to the holding register telling it to load the new data word. After the data have been transferred from the shift register to the holding register, the shift registers are cleared by being loaded with logic ones. This resets the flag code check circuitry and prevents a data word that might look like the flag code from activating the check circuitry.

The other purpose of the flag code is to provide clocking information to the receiver. The flag code's pattern of zeros and ones forms an 80 MHz square wave. This wave is presented to a phase locked loop that locks onto this frequency and produces a wave of double the frequency (160 MHz). The 160 MHz signal is used for clocking the shift register.

The holding register holds the data at the inputs of the digital to analog converter. The converter is an Analog Devices AD9768 ultra high speed converter. It features ECL logic levels, a 100 MHz update rate, and a 5 nanosecond settling time. This converter is not clocked. It continually updates its analog output according to the current digital input. The output of the D/A converter is then integrated to reproduce the original video signal. This converter/integrator pair is the same pair used in the transmitter feedback path. The output of the integrator is impedance matched to 75 ohms.

PHASE LOCKED LOOP

A phase locked loop (PLL) is basically an electronic servo loop consisting of a phase detector, a low-pass filter and a voltage controlled oscillator. The controlled oscillator phase makes it capable of locking in or synchronizing with an incoming signal in both frequency and phase. If the phase changes, indicating the incoming frequency is changing, the phase detector output voltage increases or decreases enough to keep the oscillator frequency the same as the incoming frequency."[20] In this manner, the PLL will receive a signal and track it in frequency and phase.[21] The PLL designed for the FOCUS project is basically the same as described above but with several unique modifications: frequency multiplication to generate clocking signals for the rest of the receiver, very high speed operation and a multiplexed input select.

Since only one line of serial data is available for use, no continuous clock signal can be tracked to synchronize the

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receiver. As discussed earlier, an eight bit flag code is in the form of an 80 MHz square wave, and the following eight bits are data and synchronization bits. The availability of the square wave is every other eight bits. The problem of obtaining a continuous clock signal was solved by using a multiplexed input to the PLL. During the first half of the cycle, the multiplexer feeds the eight bit square wave from the input line into the PLL. On the eighth shift of information into the register, the multiplexer switches to bit nine of the shift register since the square wave is now passing this point. In this manner, the PLL sees a continuous, 80 MHz square wave to provide correct clocking for the rest of the circuit.

The input circuit of the PLL is a phase-frequency detector. The phase detector produces a positive or negative pulse whose width is proportional to the amount of phase lead or lag between the input frequency and the current PLL output frequency. Phase error information is contained in the duty cycle of the phase detector output, that is, in the ratio of output pulse width to total period.

The next stage of the PLL is a filter. By low-pass filtering or integrating the output of the detector, usable analog information for the VCO can be recovered.

The VCO was designed to idle at the same frequency as the clock on the transmitter, thereby allowing faster lock in times for the PLL. The output of the oscillator is the 160 MHz clock that is used to drive the receiver. In order to provide for this doubling of frequency from the 80 MHz input to the PLL, a divide by two circuit is used in the feedback path from the oscillator

to the phase detector.

A D-type flip-flop is used to provide an 80 MHz signal whose phase and frequency are proportional to the VCO output. It is this 80 MHz signal that is compared to the 80 MHz wave from the incoming data stream.

For the remaining discussion it will be assumed that the loop is in lock. Since the PLL is being used for clocking, a line driver is required to reduce the fan-out from five to one. This is especially important in high speed circuitry since increasing fan-out decreases circuit speed due to capacitive loading. Three outputs from the driver are used to clock other parts of the circuit, and the other two are retained for use in the PLL.

TRANSMISSION LINE THEORY

As has been previously mentioned, the transmitter and receiver were designed to operate at a 160 MHz clock rate. At this frequency, it was suggested that the circuit board traces be treated as transmission lines. With this method, reflections at line-chip interfaces could be minimized.

The important information derived from transmission line theory will be summarized here. The derivations themselves have been placed in Appendix D.

A transmission line has associated with it the dynamic parameter Z_0, the characteristic impedance. It is defined as the ratio of transient voltage to transient current at a point in the line. When a load is connected across the line, the resistance (impedance) of this load must equal the characteristic impedance

of the line or a reflection will occur.

With ECL circuits, one method of termination (loading) requires a resistor to be connected from the end of the line to a voltage V_T. This voltage is usually -2 volts.

Two common types of PC board transmission lines are microstrip and stripline, Figure 16. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards.

Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance of no less than the trace width. It was decided that one side of the circuit board should be devoted entirely to ground plane except for small areas devoted to V_T.

In order to determine the characteristic impedance for the proposed trace widths of 0.062" and 0.031", the chart of figure 17 was used. The thickness of the boards used for the transmitter and receiver was measured to be 0.06". The board composition could not be determined and was assumed to be G-10 epoxy in order to use figure 17. The following values were calculated:

$$Z_0 = 68 \text{ ohms when } W = 0.062"$$
$$Z_0 = 90 \text{ ohms when } W = 0.031"$$

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0. The ratio of the reflected voltage to the incident voltage is the reflection coefficient. The degree of reflections which can be tolerated varies in different

38
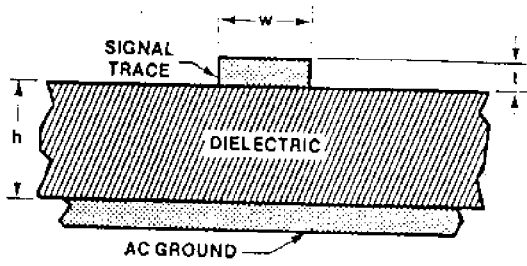
a. Microstrip

b. Stripline

Figure 16:   PC Board Transmission Lines

TRACE WIDTH — INCHES
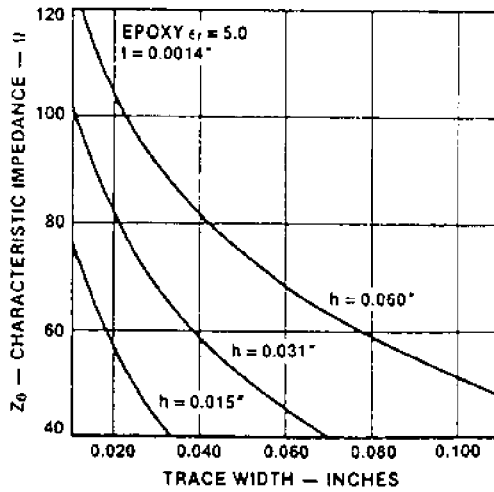
Figure 17:   Microstrip Impedance Versus   **23**
Trace Width, G-10 Epoxy

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situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs conected along the line.[6]
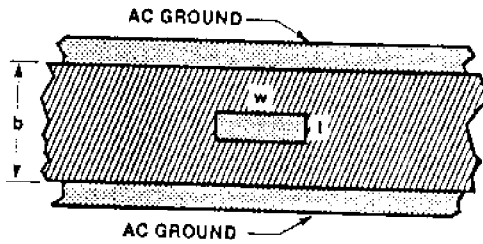
For the FOCUS design, the following constraints apply:

For Z_0 = 68 ohms, 91.8 > R_T > 50.3 ohms
For Z_0 = 90 ohms, 121.5 > R_T > 66.6 ohms

For a line terminated at the receiving end with a resistance to -2 volts, a rough rule of thumb is that the termination resistance should not exceed line impedance by more than 50%.[22]

CONSTRUCTION

In order to construct a prototype which would accurately represent the final circuit to be placed in the AMUVS, several constraints had to be met. First, the geometry of the prototype had to lend itself to layout on four inch diameter circuit boards. Second, space had to be left in the center of the design layout to accomodate the mounting bolt used in the actual AMUVS. Both Woods Hole and UNH had facilities to etch single layer, double sided boards.

The construction sequence for all the printed circuit boards followed roughly the same sequence.

1) Appropriate size boards were cut from large double sided sheets using a Dremel tool equipped with an emery cutting wheel.

2) The boards were cleaned with a non-detergent cleanser and then with ammonia to remove all surface contaminants.

3) The traces and bonding pads were layed out on the board using etch resistant transfers and tapes from DATAK.

4) The boards were then heated to 120 degrees F and a coat of photoresistive material was applied to the reverse side.

This coat was allowed to dry and the cycle was repeated two more times. This was necessary to preserve the ground plane.

5) The boards were then placed in a ferric-chloride etchant for approximately 45 minutes to remove the unwanted copper. What remained was the ground plane, signal traces and solder pads.

6) The boards were washed to stop the action of the etching process and then scrubbed to remove the tape and transfers as well as to remove the photo-resist. At this point, the boards were ready for components to be soldered on.

7) All components were soldered to the board, which was then moved to the grounded work surface for chip mounting and testing.

TESTING

After all power supply connections were made and continuity was checked, the system was powered up. The clock and analog signals were supplied by external signal generators. The clock speed was initially 100 KHz and the analog signal was a 5 KHz sine wave. The power supply was sourcing 1.2 amps of current to the transmitter (the receiver had not been constructed yet). The initial results were that no portion of the circuit appeared to be operational.

The first goal was to get the clock divider portion of the transmitter operational. The chips under consideration were the up/down counter (F100136) and the 5-input or/nor (F100101). The output of the or/nor gate was fed back to the counter to serve as load/count down control signal. Since it could not be insured that the system would come up in a state which allows a count down (high output from the or/nor), the feedback was broken and

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this input on the counter was tied to a logic high level. With this correction, the counter was locked in the count-down mode and it was operational.

All outputs of the or/nor chip were now found to be at ground potential. It was decided that, since this voltage was above logic high and the output did not change with changing inputs, the chip was faulty. When this chip was replaced, the desired output of a negative going pulse occurring once every 16 clock cycles was observed.

At this point, a check was made of the other circuit elements.

1) The A/D converter was functioning properly.

2) The hold register for the D/A converter was not operational.

3) The output of the D/A converter was at ground potential.

4) The parallel-to-serial converter was not operational. It was observed that when the load/hold control line (the output of the or/nor gate) was held low (corresponding to a load condition), the output of the A/D converter was partially ground and partially a 5 KHz sine wave.

5) The DPCM circuitry was not operational and was disconected.

The output of the A/D converter is not valid when its encode signal (clock divided by sixteen) is high. Since the hold register is essentially transparent in the load mode, these invalid signals were converted to ground potential by the D/A converter. Therefore, if the register could be made to hold

properly, then an accurate conversion could be made.

When the load/hold signal and the clock were observed simultaneously, it was clearly seen that the load/hold signal went low on a rising edge of the clock and returned to high on the next rising edge of the clock. According to the truth table for the register, load/hold had to be low while a rising clock edge occurred. The original design had counted on propagation delay to create this condition. Short line lengths and gate delays made this method unreliable. The solution was to invert the clock to all chips using this signal. (This was another reason the feedback of this signal to the up/down counter was broken: there was no way to invert the clock with respect to this signal at this chip. Inverting the clock on the counter merely shifted the pulse but did not change the phase relation between the two).

When this change was made, the output of the D/A converter was again constant at ground potential. It seemed as if progress had taken a step backwards. By looking at one of the A/D converter outputs (which showed the encode pulse envelope) and the load/hold signal simultaneously, it was observed that the load pulse arrived when data was not valid and immediately before the rising edge of the encode signal. (Recall that the encode signal is one of the inputs to the or/nor gate which produces the load/hold pulse). By using the complement of the encode signal as the input to the or/nor gate, the occurrance of the load/hold pulse was moved to the point where the converter data was valid and just before it became invalid. This method is far better than depending on delays in that it allows the converted data to

settle out before it is loaded into the register.

A check of the system at this point showed that everything except the DPCM circuit was operational. The next thing to determine was the maximum speed of the circuit. The clock speed was increased until the system was no longer functioning (no output from the D/A converter). The breakdown frequency was 15 MHz.

A check of the load/hold signal and the clock signal revealed that heavy capacitive loading due to the multiple inputs being driven was the cause of breakdown. At 15MHz, the load/hold signal could not reach a voltage low enough to be recognized as a logic low. At 20 MHz, the same happened to the clock. The solution was to add a quad driver (F100112) to the circuit.

This addition will be implemented on the second version (under construction as of 5/1/86) and is expected to make the 160 MHz rate attainable although accurate data conversion is still questionable.

The question of accuracy stems from continuing problems with the DPCM scheme. The transmitter reconstructs the input signal by integrating (low-pass filtering) the output of the D/A converter. This reconstructed signal is then subtracted from the current signal producing a difference signal which can be accurately represented by six bits. If the integrator added only a constant amount of phase shift to the signal, there would be no problem. In reality, the phase shift is a function of frequency. This causes signals at one frequency to subtract while those at another add. The end result is distortion which cannot be

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allowed. One solution under consideration is the use of constant phase shift networks to compensate the integrator phase shift.

The problems associated with the receiver have been minimal. The receiving circuitry was divided into two sections: a serial-to-parallel converter and the phase locked loop/timer. Each circuit was placed on a separate board to aid in testing the receiver.

Part of the construction plan was to have the receiver construction lag behind that of the transmiter by about a week so that problems encountered with the transmitter could be avoided in the receiver. This proved to be quite helpful.

As of May 1, the phase locked loop board has not been tested, but will be operational by the time the transmitter and the serial-to-parallel converter are capable of operating at that high a frequency. By using the trasmitter clock signal in the serial-to-parallel converter circuit, audio information was transmitted across a twisted pair transmission line.

Future cooperative efforts between WHOI and UNH include:

-- The transmission of a video signal at the clock frequency of 160 MHz.

-- Modifications to the transmitter and receiver circuitry to reduce the number of times clocking information is sent, from once every 100 nano-seconds to once every 30 milli-seconds. This would allow either the reduction of transmission rate or the addition of a second camera signal.

-- The development of a complete bi-directional telemetry system for the AMUVS.

Graded Index Fiber Terms and Characteristics

1) Fiber Structure:

Optical fibers are designed to permit light energy to travel through it in a region called the core. The light rays are prohibited from escaping because the core is surrounded by another layer of glass known as the cladding. Figure A-1 shows the geometry of the core/cladding interface. The design ot tnese glass fibers is such that the core index of refraction is larger than tne cladding index. This causes light to reflect at the boundary, and remain in the core. There are certain limitations on the maximum angle that the light can strike the core/cladding interface which must be observed to avoid losses of energy.
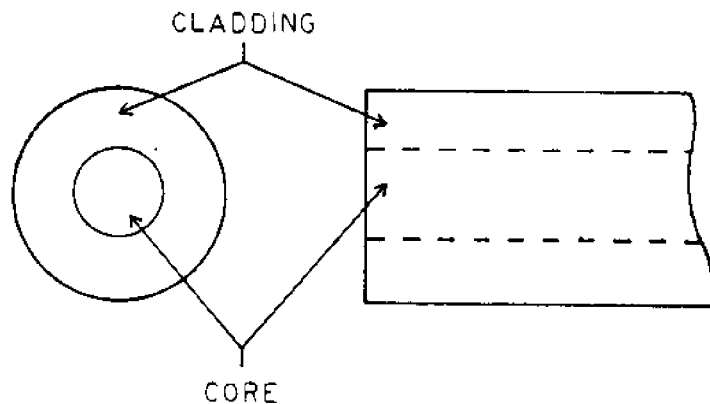
Figure A-1: Core & Cladding of an Optical Fiber

2) Transmission through an optical fiber.

Propagation of light energy in optical fibers is based on a concept of "modes". A mode is an allowable field configuration for a given geometry of a fiber. The number and type of modes allowed in a fiber determine the degree to wich tnat fiber will distort a signal. The fiber in the FOCUS system is a multimode one, as opposed to a single mode fiber. Multimode fibers are advantageous in that they can be coupled to an LED source, whereas a sinlge mode fiber requires a laser source. Multimode fibers are also easier to attach to connectors because they have a larger core dimension.

The graded index fiber operates on the principle of equalizing the group delays of the various propagating mode groups. Light rays that are traveling straight through the fiber will tend to arrive at the end faster than rays that are moving at angles and bouncing off the boundary. The varying index of refraction tends to "speed up" light traveling near the cladding, so that all the light rays arrive at the end of tne fiber at the same time. Figure A-2 shows the refractive index profile of a graded index fiber.

Efficiency of transmission is also dependent on tne wavelength of the light source. Figure A-3 shows how the attenuation of a typical multimode fiber varies with wavelength.

Other important terms dealing with fiber losses are:
Pulse Width Distortion (PWD):
This is the measure of the difference in amplitude between the input signal and the output signal (at any time t) due to
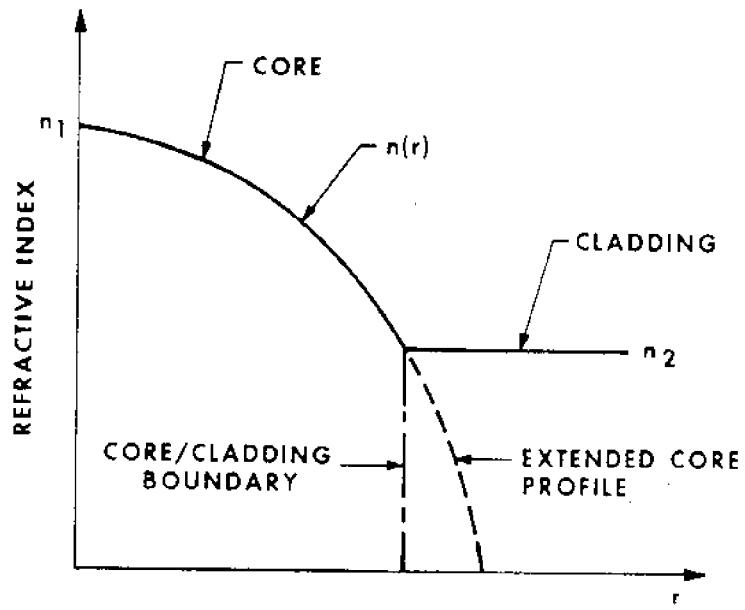
Figure A-2: Refractive Index Profile of a Graded- Inaex Fiber

Figure A-3: Spectral Loss Curve of an Optical Fiber

delays in the propagation modes (Figure A-4).

Spcetral Width( ):

Spectral Width is the range of wavelengths in the fiber. As shown in Figure A-3, broad variances in wavelength increase the overall attenuation of the signal.

INPUT SIGNAL :

FIBER

OUTPUT SIGNAL :

SLIGHTLY DISTORTED

VERY DISTORTED
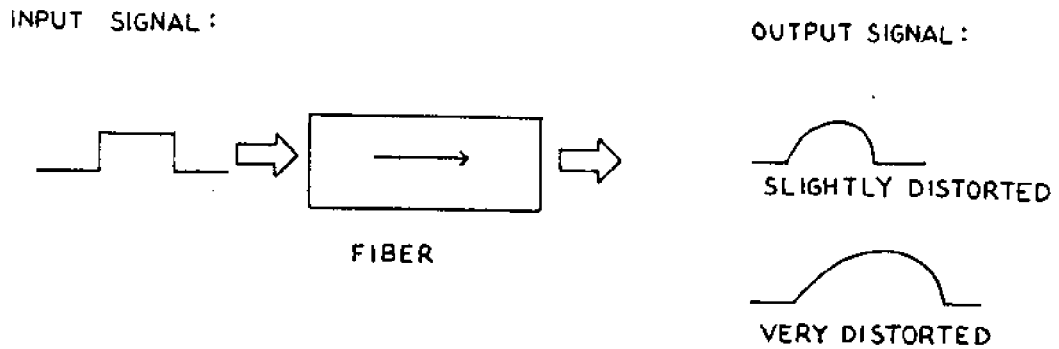
Figure A-4: Pulse Distortion of an Optical Signal Due to Delays in Propagation

Appendix B

Experimental Calculation of the Index of Refraction of the Viewport

The index of refraction of the viewport had to be determined in order to specify some of the other optical components. A laser beam was projected through the viewport, and the incident and reracted angles were measured. After several trials, Snell's law was used to calculate the index of refraction. The data for this procedure appears in Tables B-1 and B-2, and the geometry of the rigure is shown in Figure B-1.

Experiment 1 yielded an average n of 1.555, while experiment 2 produced 1.589 for the refractive index. Standard deviations were 0.0978 and 0.0867 rerspectively. Overall, the average of experiments 1 and 2 gave a refractive index n of 1.573, with a standard deviation of 0.0905. Trimming the data (i.e., disregarding the highest and lowest values) yielded n = 1.570, with a 0.0516 standard deviation. FOCUS accepted the value of n = 1.570 as the index of refraction of the viewport.

X cm	TRIAL	θ_1 INCIDENT ANGLE degrees	θ_2 REFRACTED ANGLE degrees	N VIEWPORT
.950	1	11.0	6.0996	1.7960
1.725	2	17.0	10.981	1.5354
2.750	3	27.5	17.1887	1.5630
3.050	4	31.5	18.9360	1.6106
3.640	5	36.5	22.2666	1.5703
4.011	6	40.0	24.4390	1.5541
6.320	7	64.0	35.4094	1.5517

Table B-1: Refractive Index Data, Experiment 1

X cm	TRIAL	θ_1 INCIDENT ANGLE degrees	θ_2 REFRACTED ANGLE degrees	N VIEWPORT
.850	1	8.0	5.460	1.4630
1.400	2	12.5	8.949	1.3920
2.050	3	21.0	12.985	1.5954
3.000	4	30.5	18.647	1.5880
3.800	5	41.5	23.144	1.6860
4.175	6	43.0	25.156	1.6050
5.500	7	55.0	31.744	1.5570

Table B-2: Refractive Index Data, Experiment 2
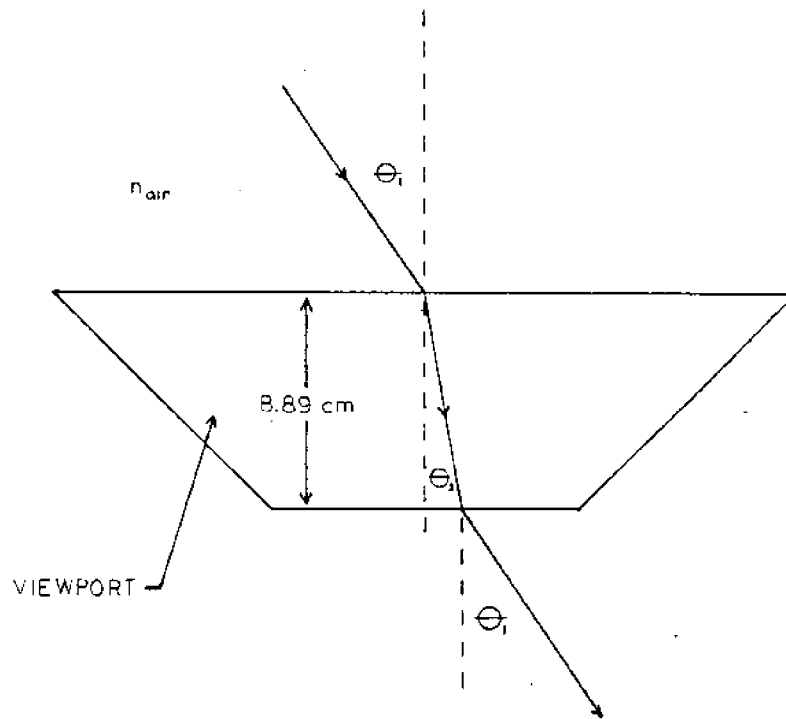
Figure B-1: Geometry of Light Passing Through the Viewport

SELFOC Lens Theory

The profile of the refactive index (Figure C- 1) is

expressed as: $n(r) = n_0\left(1 - \frac{A}{2} r^2\right)$ (1)

where $n(r)$ = refractive index at any point r,

          $n0$ = refractive index on tne optical axis z,

          A = refractive index gradient constant,

          r = radial distance from optical axis (mm).
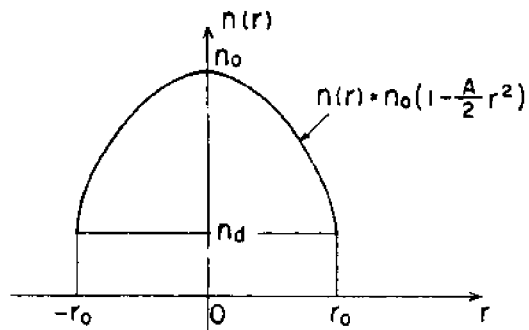
Figure C- 1: Refractive Index Profile of a SELFOC Lens

The ray matrix can be derived from equation 1:

$$
\begin{pmatrix} r_2 \\ \dot{r_2} \end{pmatrix} \begin{matrix} = \\ = \end{matrix} \begin{pmatrix} \cos \sqrt{A}\ z & \dfrac{1}{n_0\sqrt{A}}\ \sin\sqrt{A}\ z \\ -n_0\ \sqrt{A}\ \sin\sqrt{A}\ z & \cos\sqrt{A}\ z \end{pmatrix} \begin{pmatrix} r_1 \\ \dot{r_1} \end{pmatrix}
$$

where

r1 = distance between incident point and optical
axis (mm),

$\dot{r}$1 = incident angle (radians),

r2 = distance between emitting point and optical
axis (mm),

$\dot{r}$2 = emitting angle (radians),

z = length of lens (mm).

The ray matrix describes a ray passing through a lens, as shown in Figure C-2.
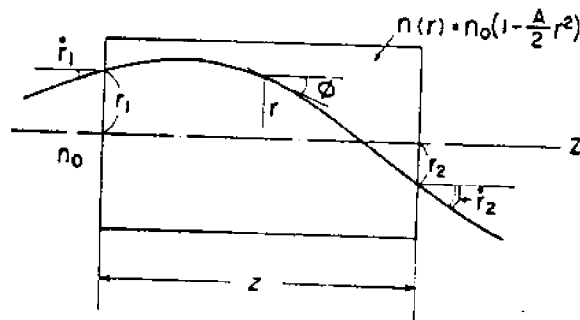
Figure C-2: A Ray Passing through a Lens

The ray matrix yields

$$r2 = r1 \cos \sqrt{A'} z,$$

when parallel light rays are incident on the lens. This results in the ray moving sinusoidally within the medium, with a period of $P = 2\pi/\sqrt{A'}$. P is often referred to as the pitch of the lens. For a collimating lens, P = 1/4.

Some important parameters of SELFOC lenses are:

1) Focal Length (f) (see Figure C-3)
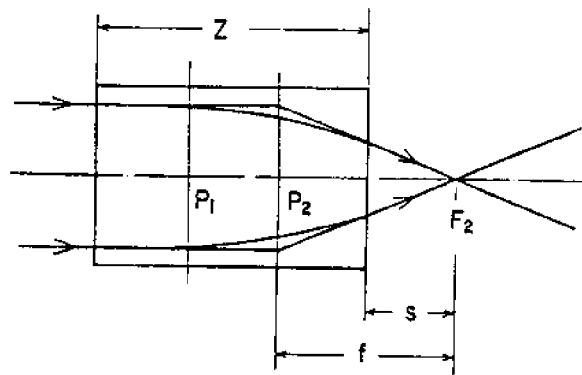
$$f = \frac{1}{n_o \sqrt{A'} \sin(-\sqrt{A'} Z)}$$

P2 = principle
point

Figure C-3: Focal Length of a SELFOC Lens

he focal length (f) is shortest for a 1/4 pitch lens.

2) Working Distance (S)

$$S = \frac{1}{n_o \sqrt{A'}} \cot\left(\sqrt{A'} Z\right)$$

The working distance S is zero for a 1/4 pitch lens.

3) Numerical Aperture (NA)   (see Figure C-4)

$$(NA)^2 = \sin^2\theta_{max} = \frac{An_o{}^2\, r_o{}^2(1-R^2)}{1-R^2 \sin^2\phi} \quad, \quad \text{where} \quad R = \frac{r}{r_o}.$$

The numerical aperture decreases as an incident ray moves away from the center axis, and is zero at the periphery.

There are two main types of SELFOC lenses: SLS and SLW. A table of parameters for the two is given on the next page (Table C-1) for a 1/4 pitch and a operating wavelength of 1300 nm.
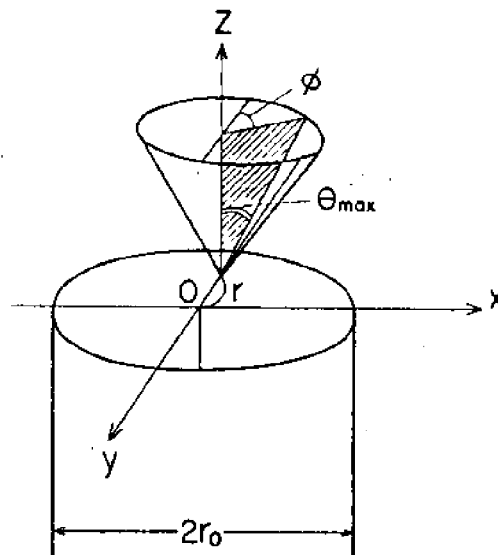
Figure C-4: Numerical Aperture of a SELFOC Lens

	(mm) DIA	$\sqrt{A}$	(mm) r_o	n_o	NA
SLS	1.0	.464	.5		
	1.5	.312	.75	1.547	.36
	2.0	.235	1.0		
SLW	1.0	.578	.5		
	1.5	.386	.75	1.595	.46
	1.8	.318	.9		
	2.0	.287	1.0		

Table C-1: Parameters for SLS and SLW SELFOC Lenses

APPENDIX D: TRANSMISSION LINE THEORY

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems.

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of the characteristic impedanced and propagation delay.

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal change or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}}$$

where L_0 = inductance per unit length, C_0 = capacitance per unit

length. Z_0 is in ohms, L_0 in henries, C_0 in farads.

A transmission line with a terminating resistor is shown in figure D-1. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0. If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.
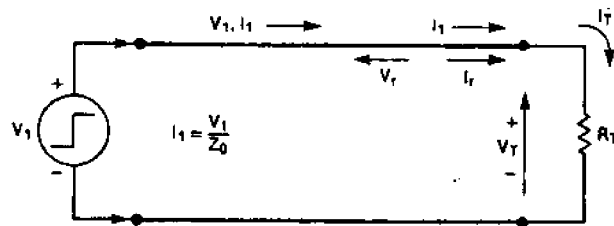
Figure D-1: Assigned polarities and directions for
determining reflections

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is

determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that ohm's low is satisfied at the line-load interface. This reflected wave starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following:

$$I_1 + I_R = I_T = \text{current into } R_T$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_R = V_T$$

Combining these two equations results in:

$$L = (R_T - Z_0)/ (R_S + Z_0) = \text{reflection coefficient}$$

With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and +1 respectively.

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_R. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S and can be calculated by replacing R_L with R_S in the equation for the reflection coefficient at the load. If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. If neither source impedance nor terminating impedance matches the characteristic impedance, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state

value with each succeeding reflection.

Terminating a line at the receiving end with a resistance equal to the characteristic impedance is called parallel termination. F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the low-state output voltage from the emitter follower. A -2 volt termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (VCC) and the VEE supply can provide the Thevenin equivalent of a single resistor to -2V if a separate termination supply is not available. The average power dissipation in the Thevenin equivalent resistors in about 10 times the power dissipation in the single resistor returned to -2 volts. For either parallel termination method, decoupling capacitors are required between the supply and ground.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure suffecient negative-going signal swing when the ECL driver swetches from the high state to the low state. The NPN emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in

voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced iss the product $I_{OH}*Z_0$.

If this product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH}*Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge.

For this application:

$R_T < 1.64*Z_0 + 3.86$ ohms.

For a line terminated at the receiving end with a resistance to -2 volts, a rough rule-of-thumb is that the termination resistance should not exceed line impedance by more than 50%.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be

longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines (Table D-2). The same considerations apply when the termination resistance is not connected at the end of the line; a section on the line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Z_0	Number of Fan-out Loads		
	1	2	4
50	1.37*	1.13	0.95
62	1.33	1.07	0.87
75	1.25	0.95	0.75
90	1.18	0.85	0.52
100	1.15	0.82	0.49

*Length in inches
Unit load = 2 pF. δ = 0.148 ns/inch

Table D-1: F100k maximum worst-case line lengths for unterminated Microstrip, distributed loading

Appendix E

AT&T ODL200 Lightwave Transmitter and Receiver

Technical Information

AT&T
ODL 200 LIGHTWAVE DATA LINK MODELS KIT INSTRUCTION MANUAL

December 1985

INTRODUCTION

The AT&T ODL 200 Lightwave Data Link Models Kit provides a means to investigate the benefits and performance of our latest lightwave data link product. The kit includes a 1252C Transmitter module, a 1352C Receiver module, and 50 feet of 62.5/125μm connectorized lightguide cable. This Instruction Manual provides an overview of the basic components and information helpful in applying fundamental applications of the lightwave data link.

BASIC COMPONENTS IN THE ODL 200 LIGHTWAVE DATA LINK MODELS KIT

Transmitter

The 1252C Transmitter is designed for data rates up to 220 Mb/s (NRZ) and provides −19 dBm peak power output. To achieve these high data rates, the transmitter uses microwave complementary bipolar integrated circuit (MCBIC) technology. It operates from either a +4.5 volt (+ Vcc) or a −4.5 volt (− VEE) power supply with a maximum supply current of 260 mA and is mounted in a 16-pin dual in-line package (DIP). The metal DIP should be grounded to provide a high degree of EMI/RFI protection. The integral lens-coupled optical connector used by the transmitter mates with an AT&T ST™ Series Multimode Fiber Optic Connector.

In addition to a long-wavelength, high-speed light-emitting diode (LED), the transmitter consists of a silicon integrated circuit and several discrete components. The transmitter is fully compatible with 100K ECL input data and produces binary 1320 nm optical output signals. All driver and bias circuits for the transmitter's InGaAsP high-radiance LED are included in the transmitter package (Figure 1). To minimize turn-on delay, the LED is biased at a small current in the off condition.

TRANSMITTER
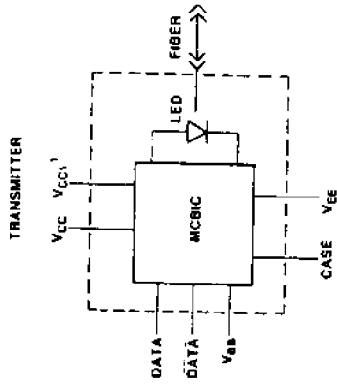
Note 1 V_{CC1} − LED Supply Voltage normally set equal to V_{CC}

Figure 1

1

Differential data is the normal input signal; however, single-ended signals can be used by connecting pin 8 (V_{BB}) to the unused data input or data input (pin 10 or 12, respectively). Pin locations are shown in Figure 2.
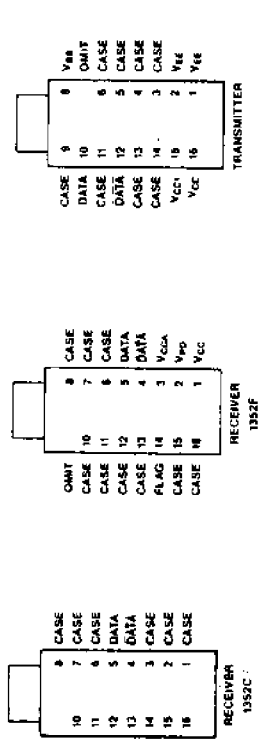
Figure 2

A recommended wiring schematic for the 1252C transmitter is indicated in Figures 3A and 3B. A maximum case temperature of 70°C is suggested. The user should utilize a sound microwave wiring layout technique and provide a ground plane on the component side of the printed wiring board, under the module. The use of sockets is detrimental. Bypass components should be located as close to the module as possible.
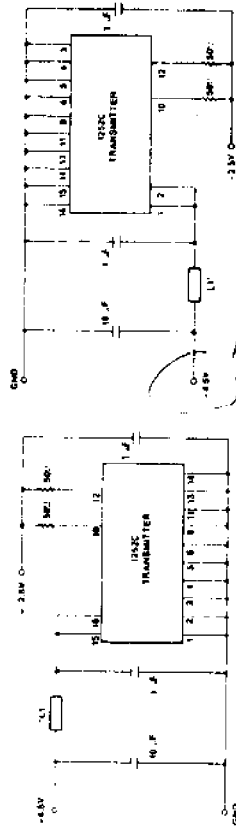
Figure 3A

Figure 3B

Receiver

The 1352C Receiver, shown in Figure 4, includes circuit technology similar to that in the 1252C Transmitter. The design consists of a transimpedance preamplifier following the PIN photodiode, a postamplifier, decision circuits, and logic output stages. The PIN photodetector diode provides the receiver with an overall peak power sensitivity of −29 dBm at a bit error rate of 10^{-9}. The receiver is designed to operate for data rates up to 220 Mb/s.

Figure 4

The 1352F receiver requires a +4.5 volt (+V_{CC}) power supply and the 1352C receiver a −4.5 volt (−V_{EE}) power supply. Both operate with a maximum current of 150 mA. A maximum case temperature of 70°C is suggested. A recommended wiring schematic for each receiver is indicated in Figures 5A and 5B. The user should utilize a sound microwave wiring layout technique and provide a ground plane on the component side of the printed wiring board, under the module. The use of sockets is detrimental. Bypass components should be located as close to the module as possible.

To maintain maximum sensitivity, the negative supply must be quiet electrically with respect to ground, which is helped by the recommended filtering. Regardless of the amplitude of the power supply noise voltage, the slew rate (dV/dT) at the V_{EE} pins (pins 15 and 16, Figure 5B) should be less than 0.25 V/μs.
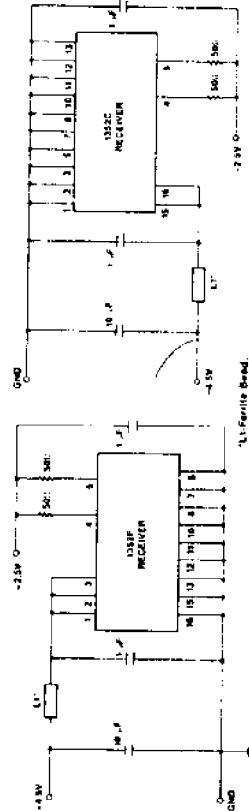
Figure 5A

Figure 5B

A high degree of EMI/RFI protection is provided by the grounded metal DIP-type receiver package; however, under adverse conditions, precautions should be taken to ensure the input signals and power supply are "clean."

The signal threshold, at pin 12 (Figure 2), provides an indication of an optical signal level. The logic "zero" state at pin 12 is used to flag a low or no optical input signal. During flagged threshold signal conditions, erroneous outputs can be disregarded.

Lightwave Apparatus and Hardware

The multimode graded index lightguide cable included in the Models Kit provides a wide range of applications along with an upgrade capability for the future. The fiber consists of a 62.5 μm diameter Ge-doped silica core that provides a numerical aperture of 0.29. The outside diameter of the fiber is 125 μm. The fiber is covered with a polyvinyl chloride (PVC) buffer jacket for abrasive damage and corrosive protection, followed by another jacket which includes KEVLAR* fiber strength members and an outer jacket (2.4 mm outside diameter) of PVC (Figure 6).

COATED FIBER

0.035" PVC (0.89 mm) OD

KEVLAR 4 x 1420 DENIER

0.095" PVC (2.4mm) OD
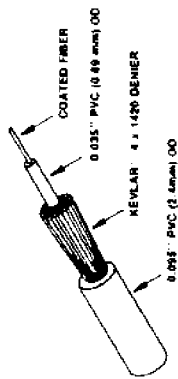
Figure 6

* Registered trademark of E. I. DuPont deNemours Co., Inc.

The connectors used are the *ST* Series Connectors. They provide a low-loss connection with stable performance. The precision design allows for quick and easy installation and ensures accurate alignment of the fiber over a wide range of temperature and humidity. The connector is applicable wherever 125-micron OD fiber is used, such as local area networks, telecommunication networks, premises distribution, or computer connections.

All tools, supplies, and instructions needed to field-mount connectors are supplied in a 1032A Tool Kit. Replacement parts used in this kit can be obtained in the D-181338 Kit.

The appropriate plug to interface with the ODL 200 is the P2020A-C-125 (Figure 7). Couplings, which are useful items for lightwave data link installations, are not provided in the Models Kit. However, the P2020A-C-125 Connector plug will mate with three different couplings which include: Bayonet/Flange C2000A-1, Bayonet/Threaded C2000A-2, and Bayonet/Floating C2000A-3 (Figure 8). These couplings provide for varied needs of connecting lightwave cable.

KEY

P2020A-C-125 CONNECTOR PLUG
(BAYONET 125 μm)

.33"
8.4 mm

.40"
10.2 mm

.89" (22.6 mm)

.0984"
2.5 mm
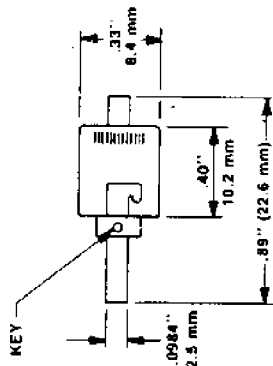
Figure 7

DATA LINK DESIGN

Mounting and Handling

The transmitter and receiver modules are designed for direct circuit board mounting. The maximum lead soldering temperature is 226°C for 10 seconds. Care should be taken when bending any of the electrical leads. The user should not create any stresses where a lead enters the transmitter package. It is not necessary to allow extra clearance between the circuit board and the output connector. However, the location of the transmitter on the circuit board must permit installation of the connectorized lightguide cable while maintaining the recommended bend radius (refer to the Installation Considerations section).

The following procedures are recommended for manually soldering the modules onto a printed wiring board. The modules should be inserted into the board. Flux may be applied to the leads or it may be contained in the solder. A mildly-activated, rosin-type flux is recommended. A solder with a tin-lead composition of 60/40 is recommended. Manual soldering should be performed with no more than a 45-watt soldering iron with a tip temperature not to exceed 357°C.

After soldering, the board should be cleaned to remove flux, flux-reaction products, and solder particles. Cleaning should be confined to the soldered side of a board. Chlorinated hydrocarbons such as 1, 1, 1-Trichloroethane or Perchloroethylene may be used as long as there is not direct application of the solution to the component on the component side of the board. Isopropyl alcohol is also acceptable. Some solvent can reach the component side of the board through unused holes, etc. It is acceptable for isolated droplets of solvent to fall on the modules.

Special handling of the modules is not required; however, they are precision devices and should be handled as such. Dirt or dust in the connector or on the lens of the transmitter or receiver can cause optical power loss. The cover for the connectors should be left in place whenever the lightguide cable is disconnected.

Installation Considerations

Installation procedures for lightguide cable actually differ little from the procedures used for small gauge electrical wire. The lightguide cable used in the optical data link is designed for indoor, or controlled environment, use. It can withstand repeated handling such as experienced in offices where rearrangement of facilities is a frequent occurrence. Installation in ducts and conduit or direct installation in walls, ceilings, and floors is possible.

The lightguide cable specifications which are important for installation are:

Tensile strength (min)	50 k psi
Ambient temperature	–32 to +68°C
Bend radius (recommended)	1.5 inch
Bend radius (min)	0.5 inch

7

C2000A-1 COUPLING
(BAYONET FLANGE)

C2000A-2 COUPLING
BAYONET THREADED

C2000A-3 COUPLING
(BAYONET FLOATING)

Figure 8

6
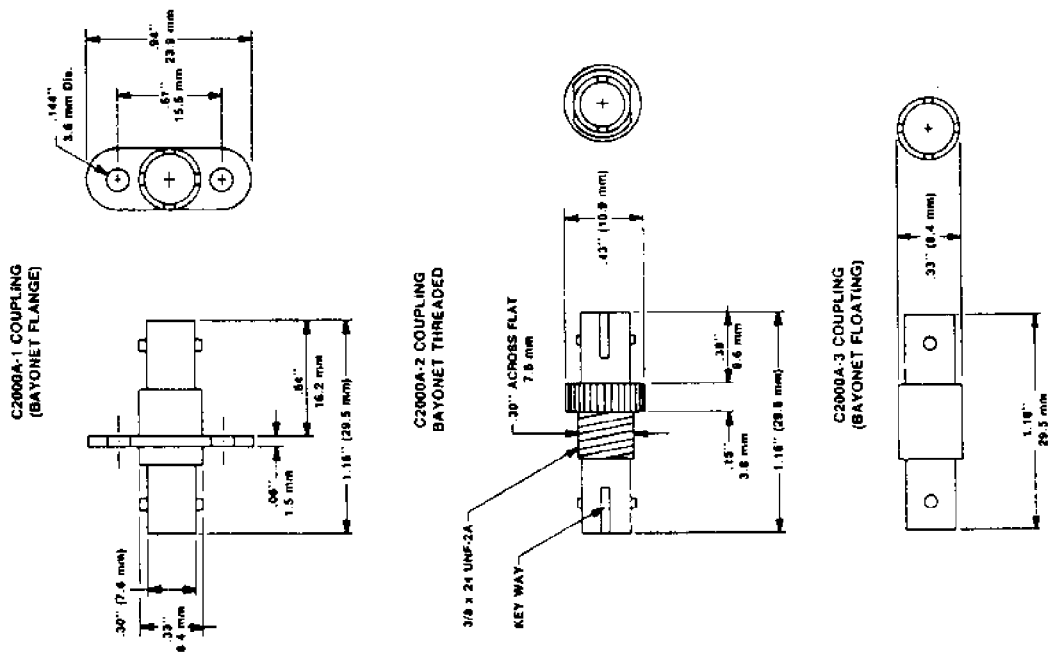
ELECTRICAL CHARACTERISTICS
ODL 200 Transmitter
(Vcc − Vee = 4.2 to 4.8 V; Operating Temperature: 0 to 70°C[1])
(Complementary Inputs[2])

Parameter	Symbol	Min	Max	Unit
Input Data Voltage—Low[3] Input Data Voltage—High[3]	VIL VIH	−1.810 −1.165	−1.475 −0.880	V V
Input Current—Low[4] Input Current—High[5]	IIL IIH	0.5 —	— 0.350	μA mA
Reference Voltage[6]	VBB	−1.396	−1.244	V
Input Transition Time[7,8]	TIN	—	1.0	ns
Power Supply Current	ICC	—	260	mA
Data Rate [NRZ Encoding]	DR	40	220	Mb/s
Peak Optical Power (Typical Conditions[9])	POH	28 (−15.5)	—	μW (dBm)
Optical Output[10] High Low	POH POL	12.5 (−19) —	88 (−10.5) POH/20 (POH −13)	μW (dBm) μW (dBm)
Output Rise Time[7,8] Output Fall Time[7,8]	tR tF	— —	1.8 2.2	ns ns
Pulse Width Distortion[8,11]	PWD	—	0.5	ns
Optical Wavelength	λ	1300	1350	nm
Spectral Width [FWHM]	$\Delta\lambda$	—	170	nm
Power Dissipation[12]	PDISS	—	1.3	W

NOTES:
1. Refer to package thermal characteristics, p. 3.
2. These specifications assume the use of both inputs with complementary input data. Similar performance can be achieved when driven single-ended.
3. Measured from VCC with a 50 Ω load to [VCC −2.0] V.
4. Measured with VIL min.
5. Measured with VIH max.
6. Measured from VCC.
7. Between 10% and 90% points.
8. Specified at a 200 Mb/s data rate. At lower data rates the maximum value scales inversely with the decrease in data rate.
9. Value given is typical, not minimum.
10. Measured peak power coupled into 0.29 NA, 62.5/125 micron fiber at +40°C. Includes power supply and end-of-life (EOL) variations.
11. The PWD as measured with an input signal having negligible PWD.
12. With 4.8 V power supply and 50% duty cycle.

E-5

ELECTRICAL CHARACTERISTICS
ODL 200 Receiver

(Vcc [1352F] – VEE [1352C] = 4.2 to 4.8 V; Operating Temperature: 0 to 70°C[1])
(Complementary Outputs[2])

Parameter	Symbol	Min	Max	Unit
Output Data Voltage – Low[3,4]	VOL	−1.810	−1.620	V
Output Data Voltage – Low[3]	VOL	−1.830	−1.605	V
Output Data Voltage – High[3,4]	VOH	−1.025	−0.880	V
Output Data Voltage – High[3]	VOH	−1.035	−0.870	V
Current Drain on VCC	ICC	−	150	mA
Current Drain on VPD	IPD	−	75	μA
Current Drain on VCCA[5]	ICCA	−	30	mA
Data Rate [NRZ Encoding]	DR	40	220	Mb/s
Optical Sensitivity – Typical Operating Conditions[6]	PIN	0.8 (−31)	−	μW (dBm)
Optical Sensitivity – Worst Case[7]	PIN	1.1 (−29.5)	−	μW (dBm)
Maximum Input Power	PMAX	−	88 (−10.5)	μW (dBm)
Optical Wavelength for Rated Sensitivity	λ	1275	1375	nm
Pulse Width Distortion[8,9]	PWD	−	1.2	ns
Output Rise Time[9,10]	tR	−	1.4	ns
Output Fall Time[9,10]	tF	−	1.4	ns
Power Dissipation[11]	PDISS	−	.750	W
Flag – Low[12]	VFL	−1.830	−1.605	V
Flag – High[12]	VFH	−1.035	−0.870	V

NOTES:
1. Refer to thermal characteristics, p. 5.
2. Specifications assume the use of both outputs with complementary data. Similar performance can be achieved using either output individually.
3. The 1352C is measured from ground with a 50 Ω load to −2.0 V. The 1352F is measured from VCCA with a 50 Ω load to VCCA −2.0 V.
4. With a 4.5 V power supply.
5. With 50 Ω loads on Data and $\overline{Data}$ to [Vcc −2.0] V (1352F), to −2.0 V (1352C).
6. Value given is typical, not minimum.
7. Peak power coupled from a 0.29 NA, 62.5/125 micron fiber at 220 Mb/s for a bit error rate of 10^{-9} at +40°C. Includes EOL.
8. The PWD as measured with a −18 dBm input signal having negligible PWD.
9. Specified at a 200 Mb/s data rate. At lower data rates the maximum value scales inversely with the decrease in data rate.
10. Between 20% and 80% points with a 50 Ω load to [Vcc −2.0] V.
11. With 4.8 V power supply, 50% duty cycle and logic outputs terminated in 50 Ω to Vcc −2 V.
12. Measured from Vcc with a 50 Ω load to [Vcc −2.0] V.

Appendix F

Transmitter and Receiver

Block Diagrams, Schematics and Timing Diagrams
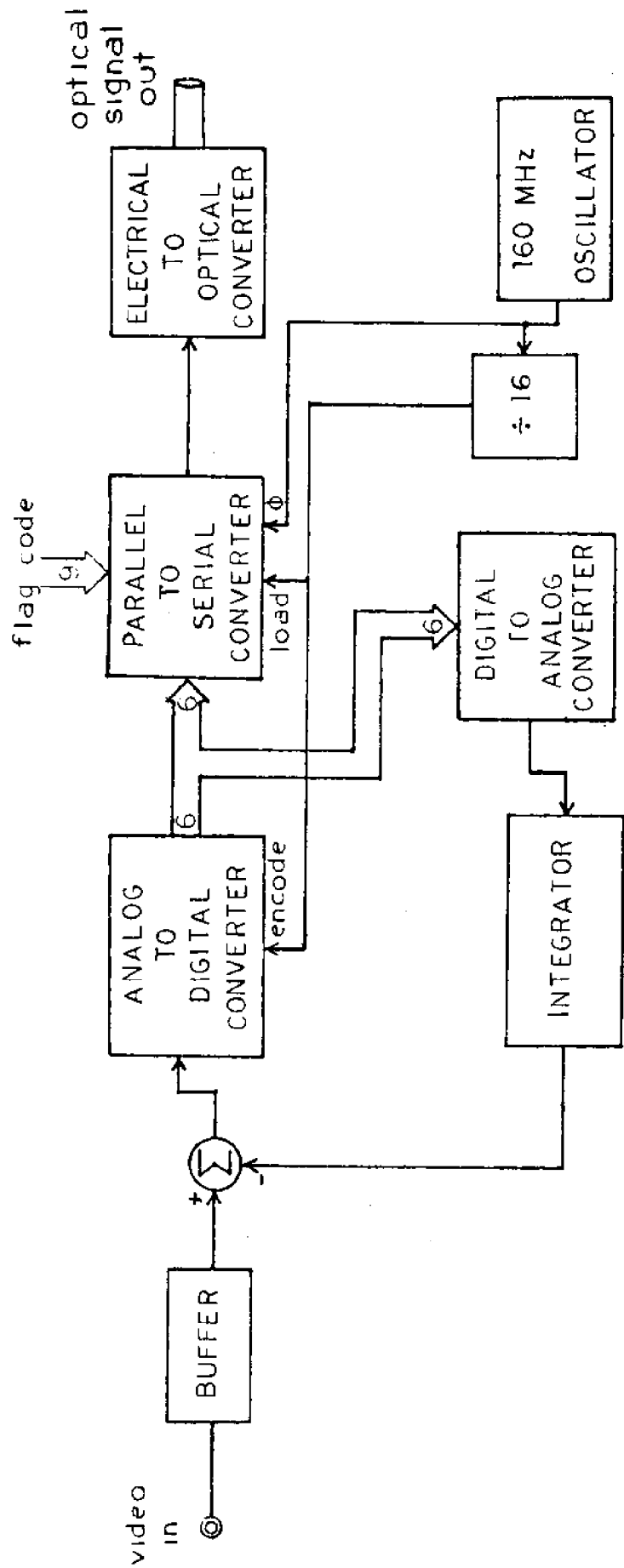
TRANSMITTER BLOCK DIAGRAM

F-1
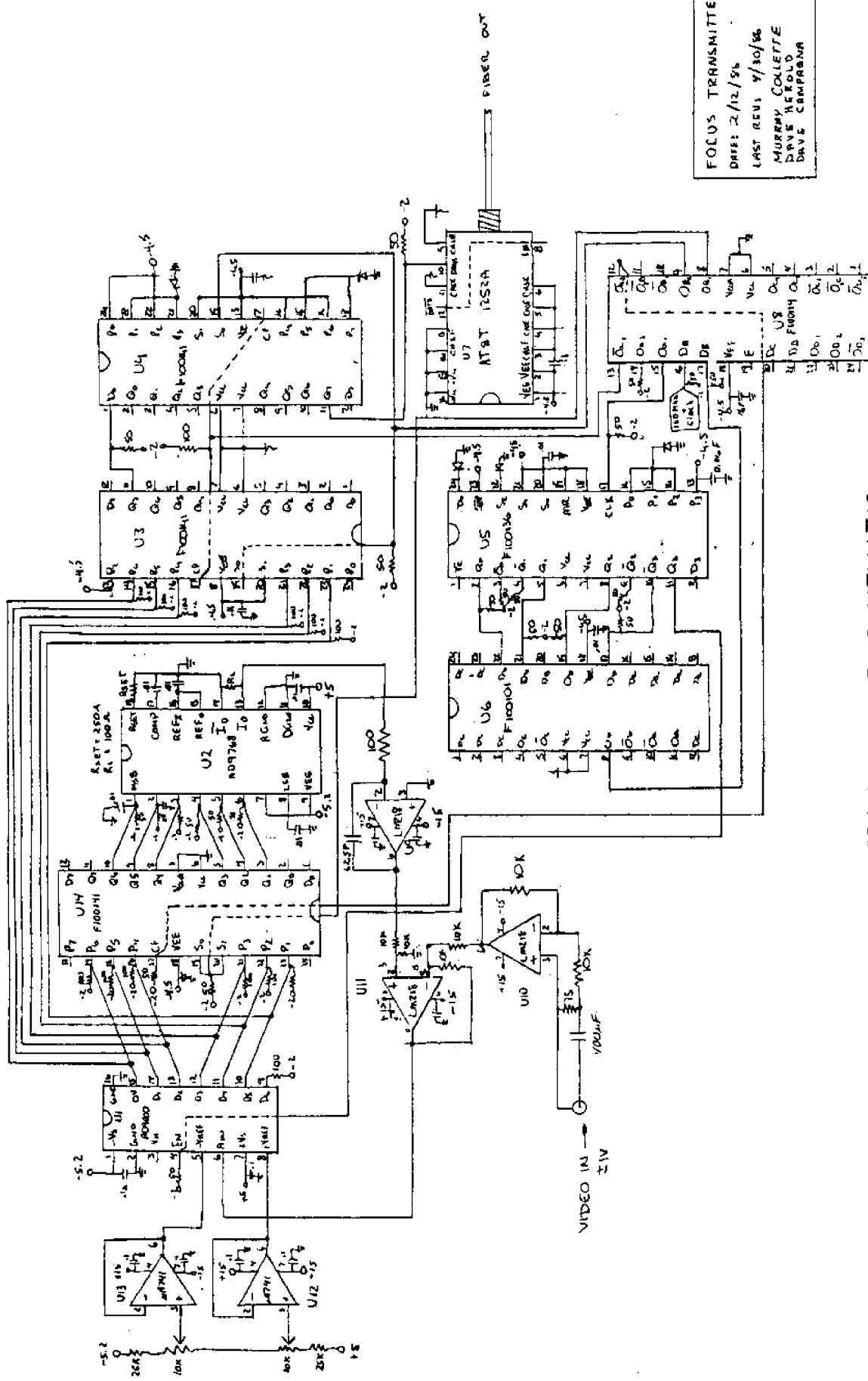
FOCUS TRANSMITTER

DATE: 2/12/96
LAST REV: 4/30/96

MURRAY COLLETTE
DAVE HEROLD
DAVE CAMPAGNA

TRANSMITTER SCHEMATIC

F-2

COUNTER VALUE (U8) 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9

CLK

$\overline{CLK}$

CONVERT. (U5-11)

A/D DIGITAL OUTPUT   NOT VALID   VALID

DATA LOAD / HOLD (U6-8)

FLAG CODE

SHIFT OUT (U4-11)   0 0 | D0 | D1 | D2 | D3 | D4 | D5   0 1 0 1 0 1 0 0 0 | Do
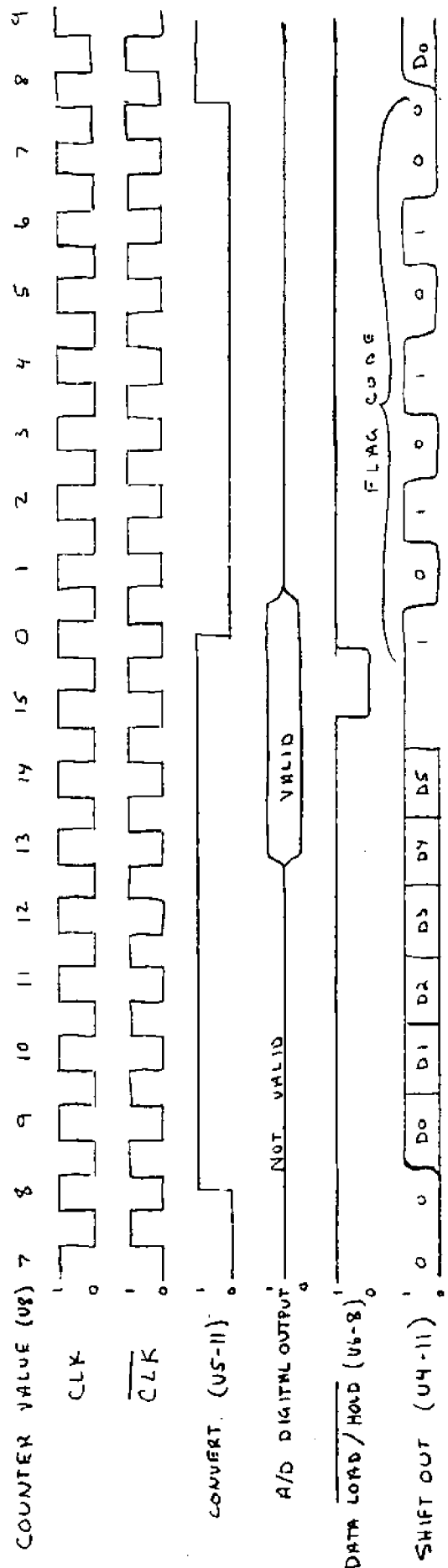
TRANSMITTER TIMING DIAGRAM

F - 3

RECEIVER BLOCK DIAGRAM

F-4
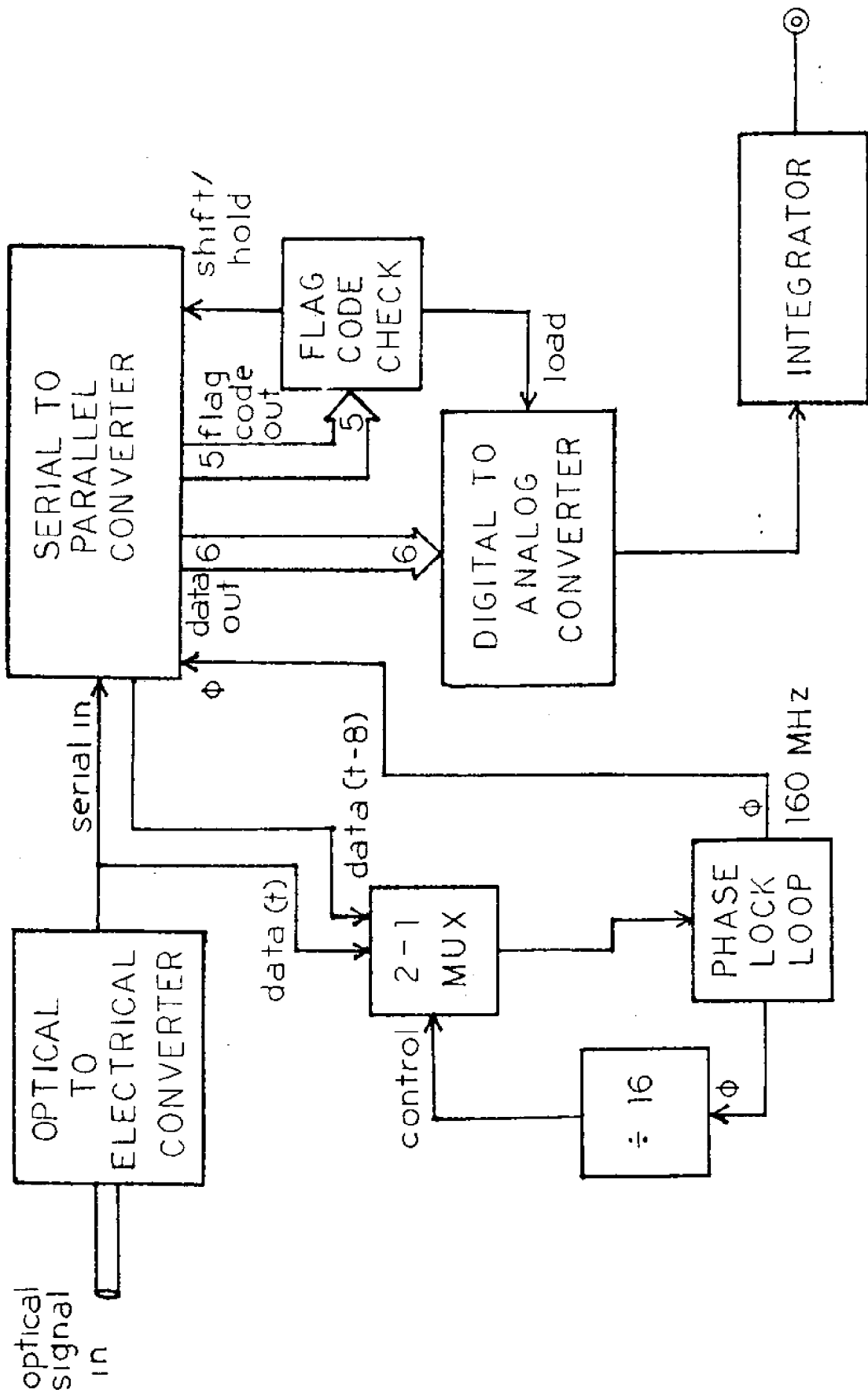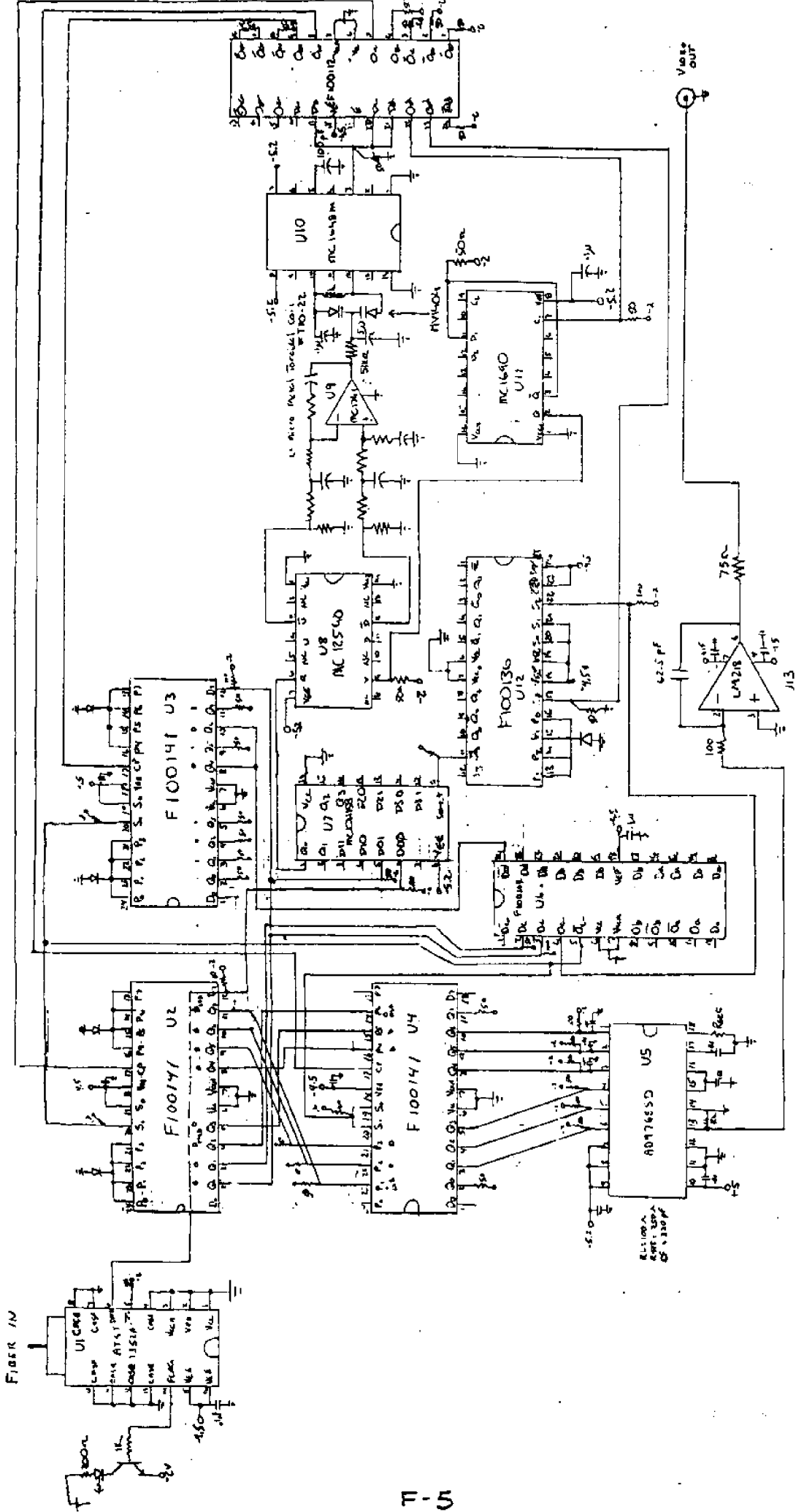
RECEIVER, PHASE LOCKED LOOP SCHEMATIC

F-5
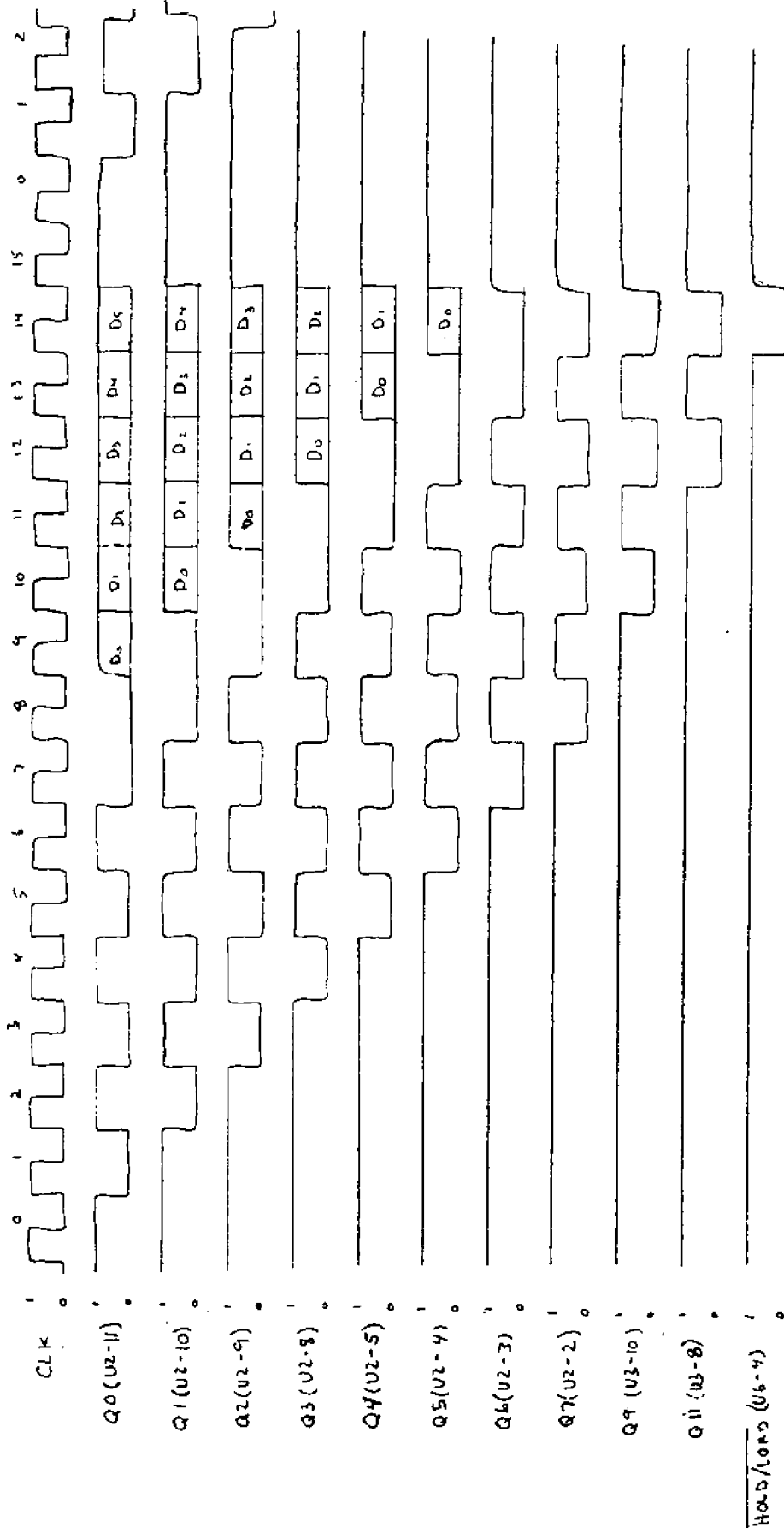
RECEIVER TIMING DIAGRAM·

F-6

SERIAL DATA IN
MUX LINE ONE
(U1-6)

DATA   DATA

MUX LINE TWO
(U3-11)

MUX SELECT
÷ 16 OF VCO
OUT (U12-11)

MUX OUT
PLL INPUT
(U8-6)

TRACKING
SIGNAL ÷ 2
OF VCO (U11-2)

LEAD ERROR
VOLTAGE (U8-3)

LAG ERROR
VOLTAGE (U8-12)

VCO CONTROL
VOLTAGE (U9-6)

4v
3v
2v
1v
0v

VCO OUTPUT
(160 MHz) (U10-3)
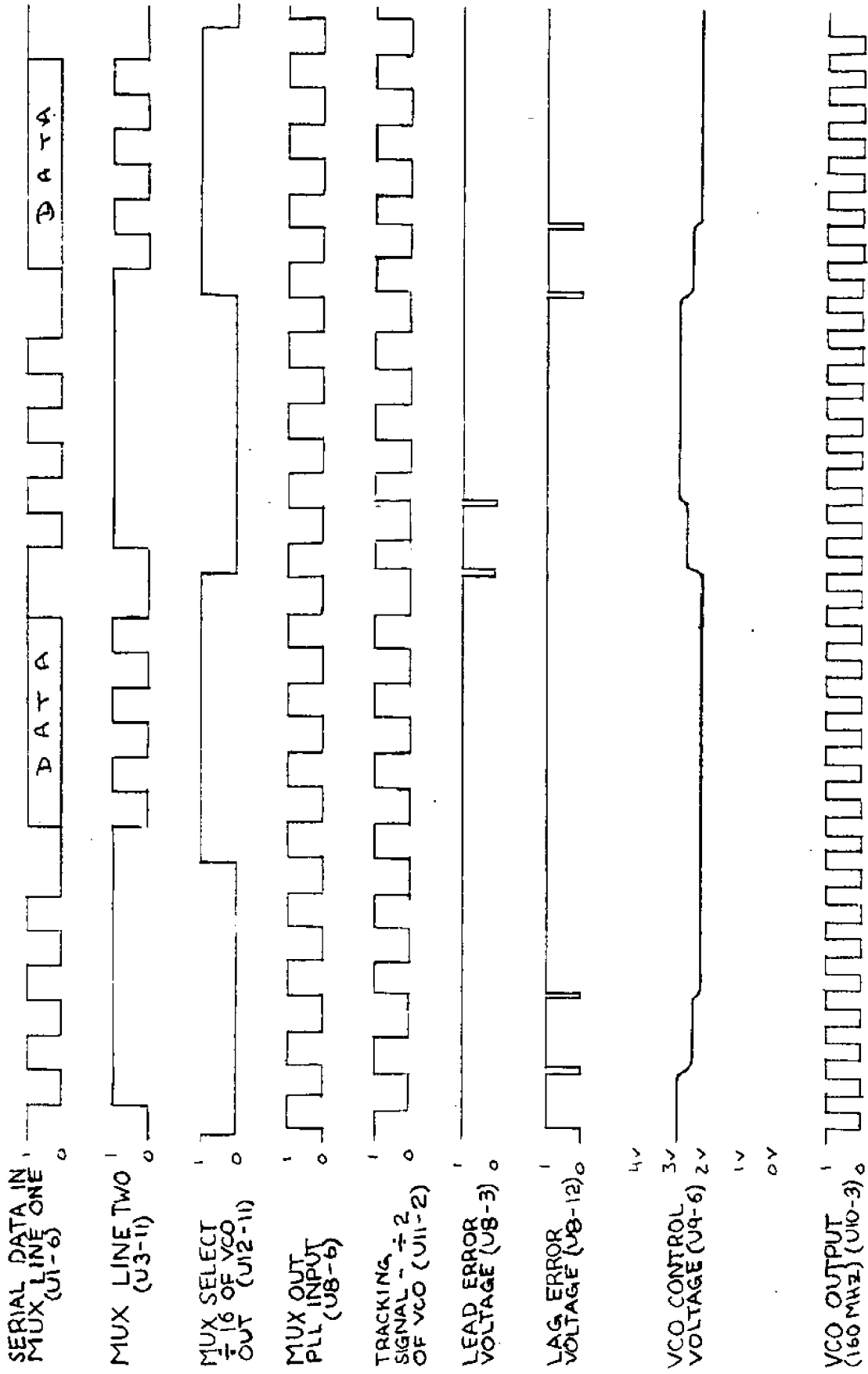
PHASE LOCKED LOOP TIMING DIAGRAM

Appendix G [28]

Data Sheets

F100K DC Family Specification

DC characteristics for the F100K series family parametric limits listed below are guaranteed for the entire F100K ECL family unless specified on the individual data sheet.

Absolute Maximum Ratings: Above which the useful life may be impaired [1]

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	0°C to +150°C
Case Temperature Under Bias (T_C)	0°C to +85°C
V_EE Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_EE to +0.5 V
Output Current (dc Output HIGH)	−50 mA
Operating Range [2]	−5.7 V to −4.2 V

DC Characteristics: $V_{EE} = -4.5$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions [4]
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV	
V_{OHC}	Output HIGH Voltage	−1035			mV	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$
V_{OLC}	Output LOW Voltage			−1610	mV	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs
I_L	Input LOW Current	0.50			μA	$V_{IN} = V_{IL(min)}$

Loading with 50 Ω to −2.0 V

DC Characteristics: $V_{EE} = -4.2$ V, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions [4]
V_{OH}	Output HIGH Voltage	−1020		−870	mV	$V_{IN} = V_{IL(max)}$ or $V_{IL(min)}$
V_{OL}	Output LOW Voltage	−1810		−1605	mV	
V_{OHC}	Output HIGH Voltage	−1030			mV	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$
V_{OLC}	Output LOW Voltage			−1595	mV	
V_{IH}	Input HIGH Voltage	−1150		−880	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs
I_L	Input LOW Current	0.50			μA	$V_{IN} = V_{IL(min)}$

Loading with 50 Ω to −2.0 V

F100101
Triple 5-Input
OR/NOR Gate

F100K ECL Product

Description

The F100101 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_{na}, D_{nb}, D_{nc}	Data Inputs
O_a, O_b, O_c	Data Outputs
$\overline{O}_a, \overline{O}_b, \overline{O}_c$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP (Top View)

24-Pin Flatpak (Top View)

Logic Symbol

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

DC Characteristics: $V_{EE} = -4.8$ V, $V_{CC} = V_{CCA} =$ GND, $T_C = 0°C$ to $+85°C$, Note 3

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions 4	
V_{OH}	Output HIGH Voltage	-1035		-880	mV	$V_{IN} = V_{IH(max)}$ or $V_{IL(min)}$	Loading with 50 Ω to -2.0 V
V_{OL}	Output LOW Voltage	-1830		-1620	mV		
V_{OHC}	Output HIGH Voltage	-1045			mV	$V_{IN} = V_{IH(min)}$ or $V_{IL(max)}$	
V_{OLC}	Output LOW Voltage			-1610	mV		
V_{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810		-1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	$V_{IN} = V_{IL(min)}$	

1. Unless specified otherwise on individual data sheet.
2. Parametric values specified at −4.2 V to −4.8 V
3. The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges
4. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions

F100112
Quad Driver

F100K ECL Product

Connection Diagrams

24-Pin DIP (Top View)

24-Pin Flatpak (Top View)

Description

The F100112 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50 Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Pin Names

D_a–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

Logic Symbol

V_{CC} = Pin 8 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

DC Characteristics: V_{EE} = –4.2 V to –4.8 V unless otherwise specified. V_{CC} = V_{CCA} = GND. T_C = 0°C to +85°C.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			350	µA	V_{IN} = $V_{IH(max)}$
I_{EE}	Power Supply Current	–38	–26	–18	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = –4.2 V to –4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.50	1.15	0.50	1.15	0.55	1.30	ns	Figures 1 and 2
t_{PHL}	Data to Output								
t_{TLH}	Transition Time	0.45	1.30	0.45	1.20	0.45	1.20	ns	
t_{THL}	20% to 80%, 80% to 20%								

Flatpak AC Characteristics: V_{EE} = –4.2 V to –4.8 V, V_{CC} = V_{CCA} = GND

Symbol	Characteristic	T_C = 0°C		T_C = +25°C		T_C = +85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.50	0.95	0.50	0.95	0.55	1.10	ns	Figures 1 and 2
t_{PHL}	Data to Output								
t_{TLH}	Transition Time	0.45	1.20	0.45	1.10	0.45	1.10	ns	
t_{THL}	20% to 80%, 80% to 20%								

*See Family Characteristics for other ac specifications.

Fig. 1 AC Test Circuit

Fig. 2 Propagation Delay and Transition Times

Notes
V_{CC}, V_{CCA} = +2 V, V_{EE} = –2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All infrared outputs are tested with 50 kΩ GND

DC Characteristics: $V_{EE} = -4.2$ V to -4.8 V unless otherwise specified, $V_{CC} = V_{CCA} = $ GND, $T_C = 0°C$ to $+85°C$.

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current Data Enable			550 450	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	-106	-73	-51	mA	Inputs Open

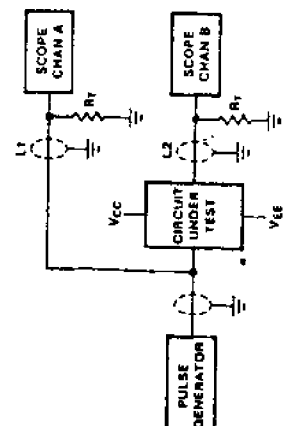## Ceramic Dual In-line Package AC Characteristics: $V_{EE} = -4.2$ V to -4.8 V, $V_{CC} = V_{CCA} = $ GND

Symbol	Characteristic	$T_C = 0°C$ Min	Max	$T_C = +25°C$ Min	Max	$T_C = +85°C$ Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.50	0.55	1.40	0.45	1.60	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	2.00	0.65	1.90	0.65	2.00	ns	Figures 1 and 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Flatpak AC Characteristics: $V_{EE} = -4.2$ V to -4.8 V, $V_{CC} = V_{CCA} = $ GND

Symbol	Characteristic	$T_C = 0°C$ Min	Max	$T_C = +25°C$ Min	Max	$T_C = +85°C$ Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.30	0.55	1.20	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	1.80	0.65	1.70	0.65	1.80	ns	Figures 1 and 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	

*See Fairney Characteristics for other dc specifications.
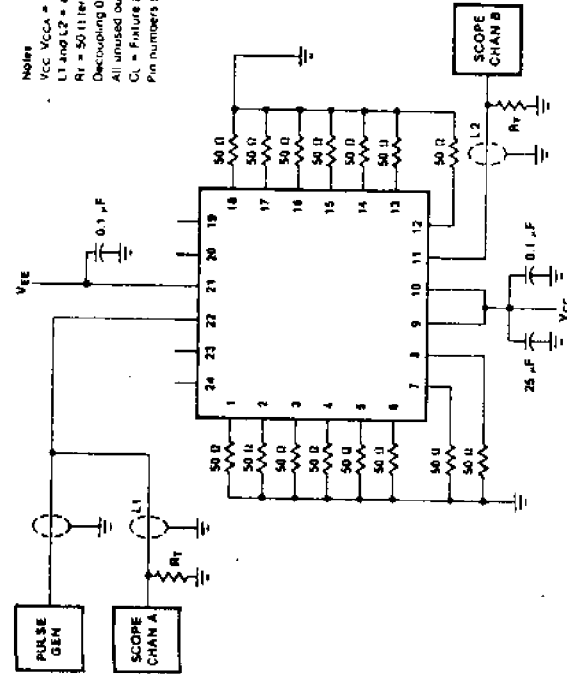
Notes
V_{CC}, $V_{CCA} = +2$ V $V_{EE} = -2.5$ V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance < 3 pF
Pin numbers shown are for Flatpak. For DIP see logic symbol

Fig. 1 AC Test Circuit

Fig. 2 Propagation Delay and Transition Times

G-4
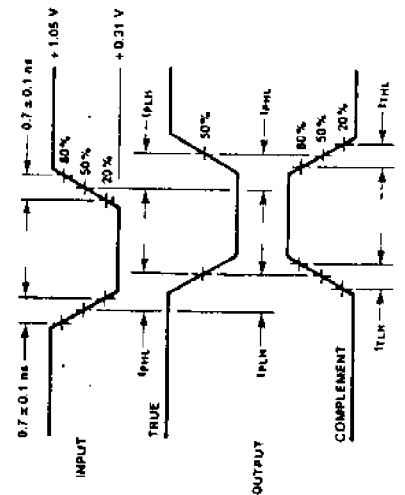
F100136
4-Stage Counter/ Shift Register

F100K ECL Product

Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable (CEP, CET) inputs are provided for ease of cascading in multistage counters. One Count Enable (CET) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count (TC) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the TC output repeats the Q_3 output. The dual nature of this TC/Q_3 output and the D_0/CET input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

Pin Names

CP	Clock Pulse Input
CEP	Count Enable Parallel Input (Active LOW)
D_0/CET	Serial Data Input/Count Enable
	Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
TC	Terminal Count Output
Q_0–Q_3	Data Outputs
$\bar{Q}_0$–$\bar{Q}_3$	Complementary Data Outputs
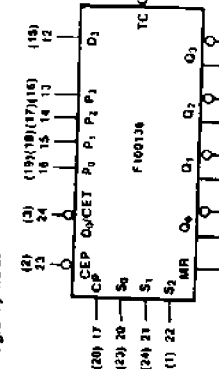
Logic Symbol

V_{CC} = Pin 8, 9
V_{CCA} = Pin 7, 10
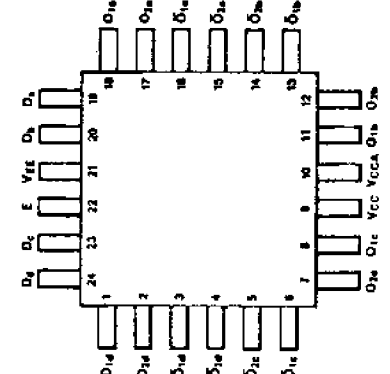V_{EE} = Pin 18, 21
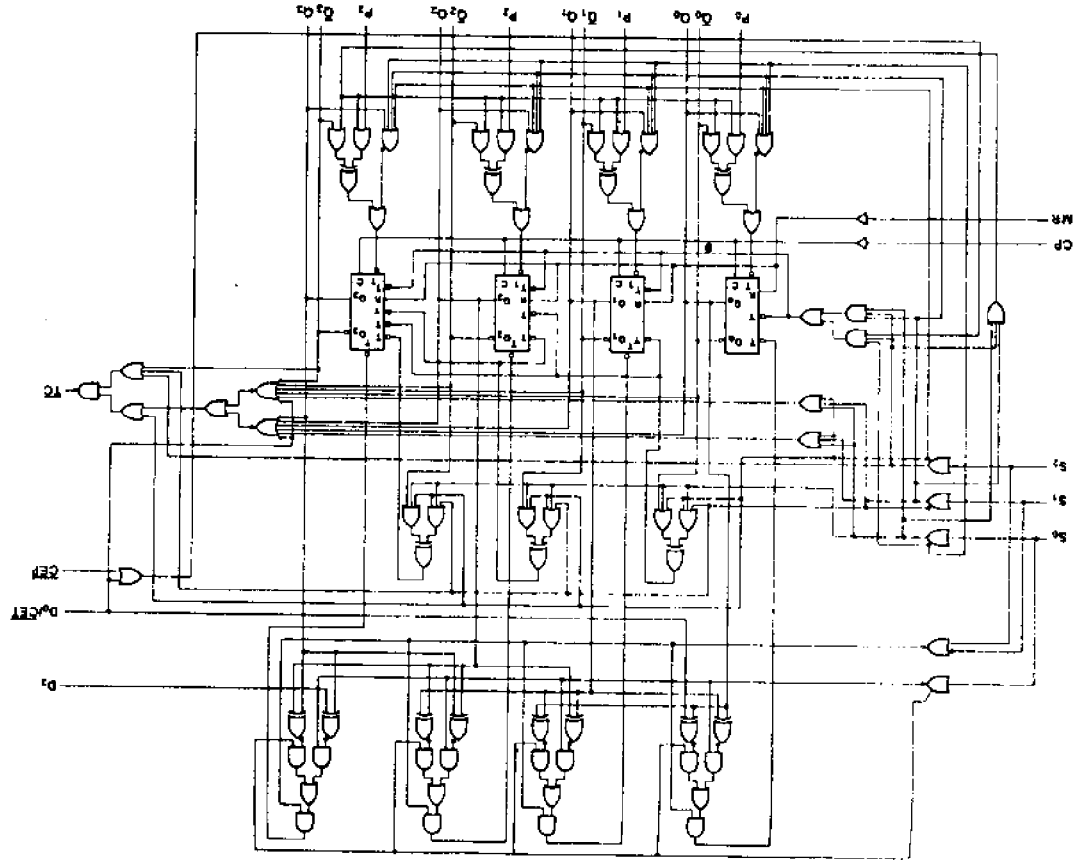
Connection Diagrams

24-Pin DIP (Top View)
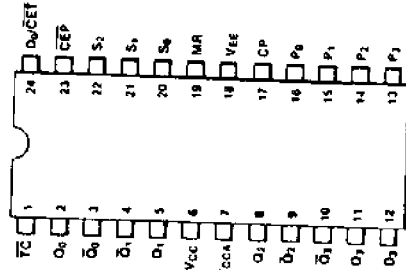
24-Pin Flatpak (Top View)

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Logic Diagram

Function Select Table

S0	S1	S2	Function
L	L	L	Parallel load
L	L	H	Count Down
L	H	L	Shift Left
L	H	H	Count Up
H	L	L	Complement
H	L	H	Clear
H	H	L	Shift Right
H	H	H	Hold

Truth Table

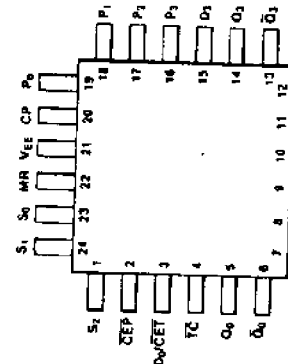| MR	S0	S1	S2	CEP	D0/CET	D3	CP	Q0	Q1	Q2	Q3	TC	Mode
L	L	L	L	X	X	X	↑	P0	P1	P2	P3	①	Preset (Parallel Load)
L	L	L	H	L	L	X	↑	(Q0-3) minus 1				①	Count Down
L	L	L	H	H	L	X	X	Q0	Q1	Q2	Q3	①	Count Down with $\overline{CEP}$ not active
L	L	L	H	X	H	X	X	Q0	Q1	Q2	Q3	H	Count Down with $\overline{CET}$ not active
L	L	H	L	X	X	D3	↑	Q1	Q2	Q3	D3	D3	Shift Left
L	L	H	H	L	L	X	↑	(Q0-3) plus 1				②	Count Up
L	L	H	H	H	L	X	X	Q0	Q1	Q2	Q3	②	Count Up with $\overline{CEP}$ not active
L	L	H	H	X	H	X	X	Q0	Q1	Q2	Q3	H	Count Up with $\overline{CET}$ not active
L	H	L	L	X	X	X	↑	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	L	Invert
L	H	L	H	X	X	X	↑	L	L	L	L	H	Clear
L	H	H	L	X	X	D0	↑	D0	Q0	Q1	Q2	Q3	Shift Right
L	H	H	H	X	X	X	X	Q0	Q1	Q2	Q3	H	Hold
L	L	L	L	X	L	X	X	L	L	L	L	L	
L	L	L	H	X	H	X	X	L	L	L	L	L	
L	H	L	L	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	H	Asynchronous Master Reset
H	H	H	H	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	L	
H	H	H	H	X	X	X	X	L	L	L	L	L	

① = L if Q0-Q3 = LLLL, H if Q0-Q3 ≠ LLLL
② = L if Q0-Q3 = HHHH, H if Q0-Q3 ≠ HHHH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

DC Characteristics

VEE = -4.2 V to -4.8 V unless otherwise specified, VCC = VCCA = GND, TC = 0°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
IIH	Input HIGH Current				µA	VIN = VIH(max)
	Pn, Sn			180		
	CEP			200		
	MR			240		
	D3			280		
	CP			390		
	D0/CET			530		
IEE	Power Supply Current	-283	-195	-136	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics

VEE = -4.2 V to -4.8 V, VCC = VCCA = GND

Symbol	Characteristic	TC = 0°C Min	TC = 0°C Max	TC = +25°C Min	TC = +25°C Max	TC = +85°C Min	TC = +85°C Max	Unit	Condition
fMAX	Shift Frequency	250		250		250		MHz	Figures 2 and 3
tPLH / tPHL	Propagation Delay CP to Qn, Q̄n	0.85	2.10	0.85	2.10	0.85	2.25	ns	Figures 1 and 3
tPLH / tPHL	Propagation Delay CP to TC	1.90	4.80	1.90	4.60	1.90	5.20	ns	Figures 1 and 3
tPLH / tPHL	Propagation Delay MR to Qn, Q̄n	1.20	2.95	1.35	2.95	1.20	3.10	ns	Figures 1 and 4
tPLH / tPHL	Propagation Delay MR to TC	2.20	4.80	2.20	4.80	2.20	5.30	ns	Figures 1 and 5
tPLH / tPHL	Propagation Delay D0/CET to TC	1.40	3.20	1.40	3.20	1.40	3.50	ns	Figures 1 and 3
tPLH / tPHL	Propagation Delay Sn to TC	1.70	4.60	1.80	4.60	1.80	5.10	ns	Figure 6
tTLH / tTHL	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	Figure 6
ts	Setup Time							ns	
	D3	1.20		1.20		1.20			
	Pn	1.70		1.70		1.70			
	D0/CET, CEP	1.45		1.45		1.45			
	Sn	3.30		3.30		3.30			
	MR (Release Time)	2.60		2.60		2.60			
tn	Hold Time							ns	
	D3	0.20		0.20		0.20			
	Pn	0.10		0.10		0.10			
	D0/CET, CEP	0.20		0.20		0.20			
	Sn	-0.90		-0.90		-0.90			
tpw(H)	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3 and 4

*See Family Characteristics for other ac specifications.

Flatpak AC Characteristics: $V_{EE} = -4.2\,V$ to $-4.8\,V$, $V_{CC} = V_{CCA} = GND$

Symbol	Characteristic	$T_C = 0°C$ Min	Max	$T_C = +25°C$ Min	Max	$T_C = +85°C$ Min	Max	Unit	Condition
f_{shift}	Shift Frequency	250		250		250		MHz	Figures 2 and 3
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	1.90	0.85	1.90	0.85	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.60	1.90	4.40	1.90	5.00	ns	Figures 1 and 3
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.75	1.35	2.75	1.20	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.60	2.20	4.60	2.20	5.10	ns	Figures 1 and 4
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.00	1.40	3.00	1.40	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	1.70	4.40	1.80	4.40	1.80	4.90	ns	Figures 1 and 5
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	Figures 1 and 3
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	1.10 1.60 1.35 3.20 2.50		1.10 1.60 1.35 3.20 2.50		1.10 1.60 1.35 3.20 2.50		ns	Figure 6
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	0.10 0 0.10 -1.00		0.10 0 0.10 -1.00		0.10 0 0.10 -1.00		ns	Figure 6
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	Figures 3 and 4

Fig. 1 AC Test Circuit

Fig. 2 Shift Frequency Test Circuit (Shift Left)

Fig. 5 Propagation Delay (Serial Data, Selects)

INPUT

OUTPUT

Fig. 6 Setup and Hold Time

INHIBIT COUNT

ENABLE COUNT

CEP

D_n, P_n, S_n

CLOCK

Notes

Fig. 3 Propagation Delay (Clock) and Transition Times

DATA

CLOCK

OUTPUT

OUTPUT

Fig. 4 Propagation Delay (Reset)

MR

CLOCK

OUTPUT

OUTPUT

G - 8

F100141
8-Bit Shift Register

F100K ECL Product

Connection Diagrams

24-Pin DIP (Top View)
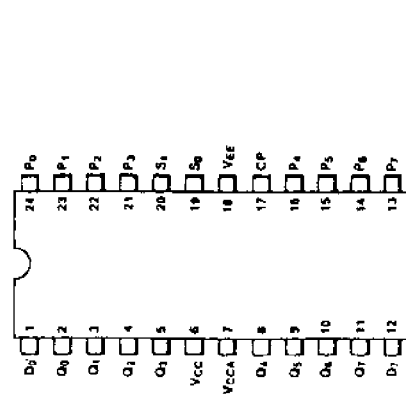
24-Pin Flatpak (Top View)
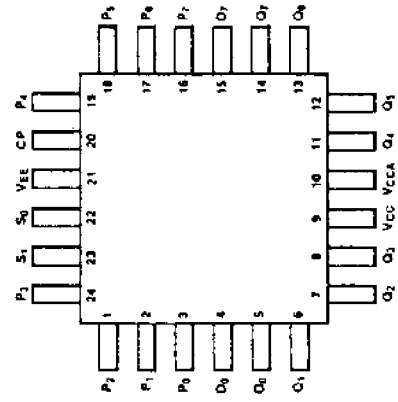
Description

The F100141 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) and parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry," "hold," "shift left" or "shift right" as described in the Truth Table.

Pin Names

CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

Logic Symbol

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 8 (21)
( ) = Flatpak

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

F100136

Application

3-Stage Divider, Preset Count Down Mode

Note
If $S_0 = S_1 = S_2 =$ LOW, then $T_C =$ LOW.

Slow Expansion Scheme

Fast Expansion Scheme

F100141

Ceramic Dual In-line Package AC Characteristics: $V_{EE} = -4.2$ V to -4.8 V, $V_{CC} = V_{CCA} = $ GND

Symbol	Characteristic	$T_C = 0°C$ Min	Max	$T_C = +25°C$ Min	Max	$T_C = +85°C$ Min	Max	Unit	Condition
f_{shift}	Shift Frequency	275		275		255		MHz	Figures 2 and 3
t_{PLH}, t_{PHL}	Propagation Delay CP to Output	0.90	2.40	1.10	2.30	1.10	2.50	ns	Figures 1 and 3
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	
t_s	Setup Time D_n, P_n / S_n	0.85 / 2.20		0.85 / 2.20		0.85 / 2.20		ns	Figure 4
t_h	Hold Time D_n, P_n / S_n	0.60 / 0.10		0.60 / 0.10		0.60 / 0.10		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

Flatpak AC Characteristics: $V_{EE} = -4.2$ V to -4.8 V, $V_{CC} = V_{CCA} = $ GND

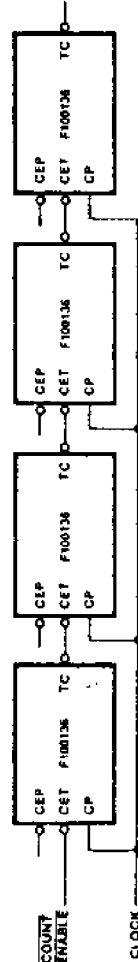| Symbol	Characteristic	$T_C = 0°C$ Min	Max	$T_C = +25°C$ Min	Max	$T_C = +85°C$ Min	Max	Unit	Condition
f_{shift}	Shift Frequency	300		300		280		MHz	Figures 2 and 3
t_{PLH}, t_{PHL}	Propagation Delay CP to Output	0.90	2.20	1.10	2.10	1.10	2.30	ns	Figures 1 and 3
t_{TLH}, t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_s	Setup Time D_n, P_n / S_n	0.75 / 2.10		0.75 / 2.10		0.75 / 2.10		ns	Figure 4
t_h	Hold Time D_n, P_n / S_n	0.50 / 0		0.50 / 0		0.50 / 0		ns	
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3

F100141

Logic Diagram

Truth Table

Function	D_7	D_0	S_1	S_0	D_n	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
			Inputs							Outputs				
Load Register	X	X	L	L	X	⌐	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	X	L	H	L	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	X	L	H	H	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	X	⌐	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	X	⌐	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	X	No Change							
Hold	X	X	X	X	X	H	No Change							
Hold	X	X	X	X	X	L	No Change							

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH transition

DC Characteristics: $V_{EE} = -4.2$ V to -4.8 V unless otherwise specified, $V_{CC} = V_{CCA} = $ GND, $T_C = 0°C$ to $+85°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_H	Input HIGH Current D_n, P_n, S_n / CP			220 / 550	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	-238	-170	-119	mA	Inputs Open

*See Family Characteristics for other DC specifications

Fig. 1 AC Test Circuit

Fig. 2 Shift Frequency Test Circuit (Shift Left)

Fig. 3 Propagation Delay and Transition Times

CLOCK

PARALLEL

OUTPUT

0.7 ± 0.1 ns

$+1.05$ V

$+0.31$ V

80%

50%

20%

t_{PLH}

t_{PHL}

t_{TLH}

t_{THL}

$1/f_{shift}$

$t_{p(H)}$

Fig. 4 Setup and Hold Times

P_n, S_n, D_n

CLOCK

$+1.05$ V

$+0.31$ V

$+1.05$ V

$+0.31$ V

50%

50%

t_s

t_h

Notes

t_s is the minimum time before the transition of the clock that information must be present at the data input

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input

Notes

VCC, VCCA = +2 V   VEE = –2.5 V

L1, L2 and L3 = equal length 50 Ω impedance lines

R_T = 50 Ω terminator internal to scope

Decoupling 0.1 μF from VCC and VEE

All unused outputs are loaded with 50 Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak. For DIP see logic symbol

PULSE GENERATOR

SCOPE CHAN A

SCOPE CHAN B

R_T

50 Ω

0.1 μF

VCC

25 μF

VEE

PULSE GENERATOR

SCOPE CHAN A

PULSE GENERATOR

SCOPE CHAN B

$+1.05$ V

50 Ω

50 Ω

R_T

R_T

50 Ω

D_0 P_0 P_1 P_2 P_3 P_4 P_5 P_6 P_7 D_7

Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

CP S_0 S_1

Notes

1 For shift right mode pulse generator connected to S_0 is moved to S_1

2 Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load

3 The feedback path from output to input should be as short as possible

3-66

MC1648/MC1648M

VOLTAGE-CONTROLLED OSCILLATOR
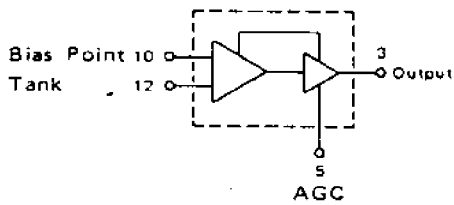
Input Capacitance = 6 pF typ

Maximum Series Resistance for L (External
    Inductance) = 50 Ω typ

Power Dissipation = 150 mW typ/pkg
    (+5.0 Vdc Supply)

Maximum Output Frequency = 225 MHz typ

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a –5.2 Vdc supply, depending upon system requirements.

Supply Voltage	Gnd Pins	Supply Pins
+5.0 Vdc	7, 8	1, 14
–5.2 Vdc	1, 14	7, 8
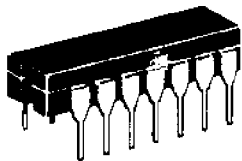
L SUFFIX
CERAMIC PACKAGE
CASE 632
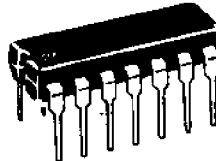
P SUFFIX
PLASTIC PACKAGE
CASE 646

F SUFFIX
CERAMIC PACKAGE
CASE 607

FIGURE 1 – CIRCUIT SCHEMATIC

Numbers in parentheses denote pin number for F package (Case 607), L package (Case 632), and P package (Case 646).

MC1648/MC1648M

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	V_IHmax (Volts)	V_ILmin (Volts)	V_CC (Volts)	I_L (mAdc)	Conditions
MC1648					
-30°C	+2.00	+1.50	5.0	-5.0	Inputs and outputs open.
+25°C	+1.85	+1.35	5.0	-5.0	V_{ILmin} to Pin 12, I_L @ Pin 3.
+85°C	+1.70	+1.20	5.0	-5.0	V_{IHmax} to Pin 12, I_L @ Pin 3.
MC1648M					V_{ILmin} to Pin 12.
-55°C	+2.07	+1.57	5.0	-5.0	
+25°C	+1.85	+1.35	5.0	-5.0	See Figure 3.
+125°C	+1.60	+1.10	5.0	-5.0	

FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT
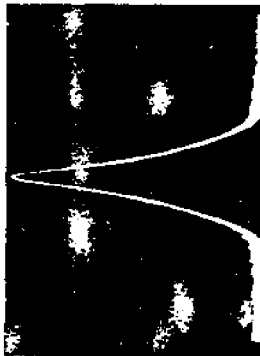
BW = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div

L: Micro Metal toroid #T20-22, 8 turns #30 Enameled Copper wire
C = 3.0 - 35 pf

+5.0 Vdc
10 µF
0.1 µF
1200*
Signal Under Test
0.1 µF

*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuation. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS
Supply Voltage = +5.0 Volts

Characteristic	Symbol	-55°C Min	-55°C Max	-30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Typ	+85°C Max	+125°C Min	+125°C Max	Unit	Conditions
Power Supply Drain Current	I_E	–	–	–	–	–	–	41	–	–	–	–	–	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	3.92	4.13	3.955	4.185	4.04	–	4.25	4.11	–	4.36	4.16	4.40	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	3.13	3.38	3.16	3.40	3.20	–	3.43	3.22	–	3.475	3.23	3.51	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	1.67	1.97	1.60	1.90	1.45	–	1.75	1.30	–	1.60	1.20	1.50	Vdc	V_{ILmin} to Pin 12.
Peak-to-Peak Tank Voltage	V_{PP}	–	–	–	–	–	400	–	–	–	–	–	–	mV	See Figure 3.
Output Duty Cycle	VDC	–	–	–	–	–	50	–	–	–	–	–	–	%	
Oscillation Frequency	f_{max}**	–	225	–	225	200	225	225	–	225	–	225	–	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	V_{IHmax} (Volts)	V_{ILmin} (Volts)	V_{CC} (Volts)	I_L mAdc
MC1648				
−30°C	−3.20	−3.70	−5.2	−5.0
+25°C	−3.35	−3.85	−5.2	−5.0
+85°C	−3.50	−4.00	−5.2	−5.0
MC1648M				
−55°C	−3.13	−3.63	−5.2	−5.0
+25°C	−3.35	−3.85	−5.2	−5.0
+125°C	−3.60	−4.10	−5.2	−5.0

ELECTRICAL CHARACTERISTICS

Supply Voltage = −5.2 Volts

Characteristic	Symbol	−55°C Min	Typ	Max	−30°C Min	Typ	Max	+25°C Min	Typ	Max	+85°C Min	Typ	Max	+125°C Min	Typ	Max	Unit	Conditions
Power Supply Drain Current	I_E	—		—	—		—	—		41	—		—	—		—	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	−1.080		−0.870	−1.045		−0.815	−0.960		−0.750	−0.890		−0.640	−0.840		−0.600	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	−1.920		−1.670	−1.890		−1.650	−1.850		−1.620	−1.830		−1.575	−1.820		−1.540	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	−3.53		−3.23	−3.60		−3.30	−3.75		−3.45	−3.90		−3.60	−4.00		−3.70	Vdc	V_{ILmin} to Pin 12.
Peak-to-Peak Tank Voltage	V_{P-P}	—		—	—		—	—	400	—	—		—	—		—	mV	See Figure 3
Output Duty Cycle	V_{DC}	—		—	—		—	—	50	—	—		—	—		—	%	See Figure 3
Oscillation Frequency	f_{max}**	—	225	—	—	225	—	200	225	—	—	225	—	—	225	—	MHz	See Figure 3

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

* Use high impedance probe (>1 0 Megohm must be used)

** The 1200 ohm resistor and the scope termination impedance constitute a 25 1 attenuator probe Coax shall be CT 070 50 or equivalent

*** Bypass only that supply opposite ground

PRF = 1 0 MHz
Duty Cycle (V_{DC}) = $\frac{t_a}{t_b}$

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback, by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that

FIGURE 4 — THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE
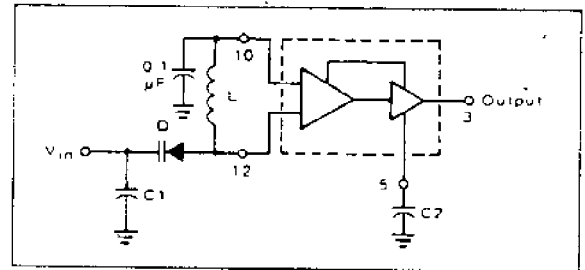
the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5

FIGURE 5 — NOISE DEVIATION TEST CIRCUIT AND WAVEFORM
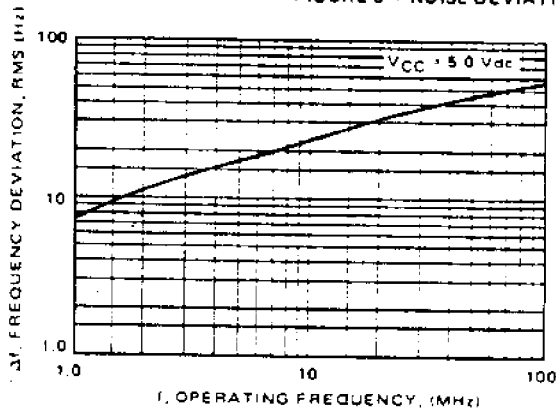
Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1 0 10	MV2115	100
10 60	MV2115	2 3
60 100	MV2106	0 15

Frequency Deviation = $\frac{(HP5210A\ output\ voltage)\ (Full\ Scale\ Frequency)}{1\ 0\ Volt}$
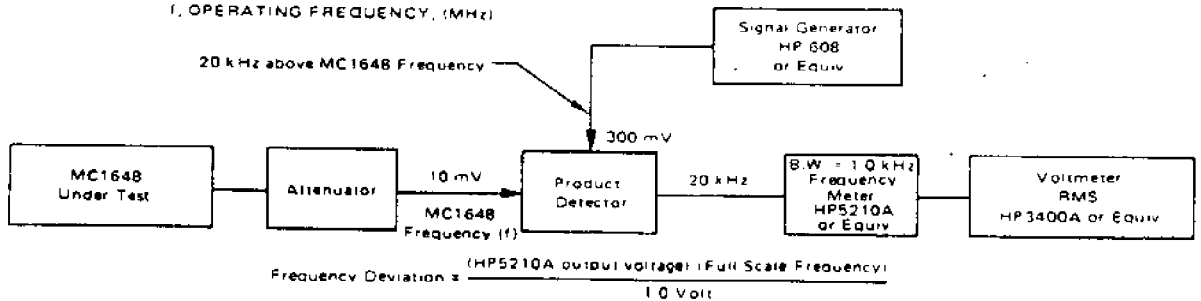
NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimized prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25°C$

FIGURE 6

L: Micro Metal Toroidal Core #T 44-10.
4 turns of No. 22 copper wire.

$V_{CC1} = V_{CC2} = +5$ Vdc
$V_{EE1} = V_{EE2} = $ Gnd

*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT 070 50 or equivalent.

FIGURE 7

L: Micro Metal Toroidal Core #T44 10
4 turns of No. 22 copper wire

$C = 500$ pF

$V_{CC1} = V_{CC2} = +5$ Vdc
$V_{EE1} = V_{EE2} = $ Gnd

*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT 070 50 or equivalent

FIGURE 8

L: Micro Metal Toroidal Core =T30 22.
5 turns of No. 20 copper wire.

$V_{CC1} = V_{CC2} = +5$ Vdc
$V_{EE1} = V_{EE2} = $ Gnd

*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT 070 50 or equivalent.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

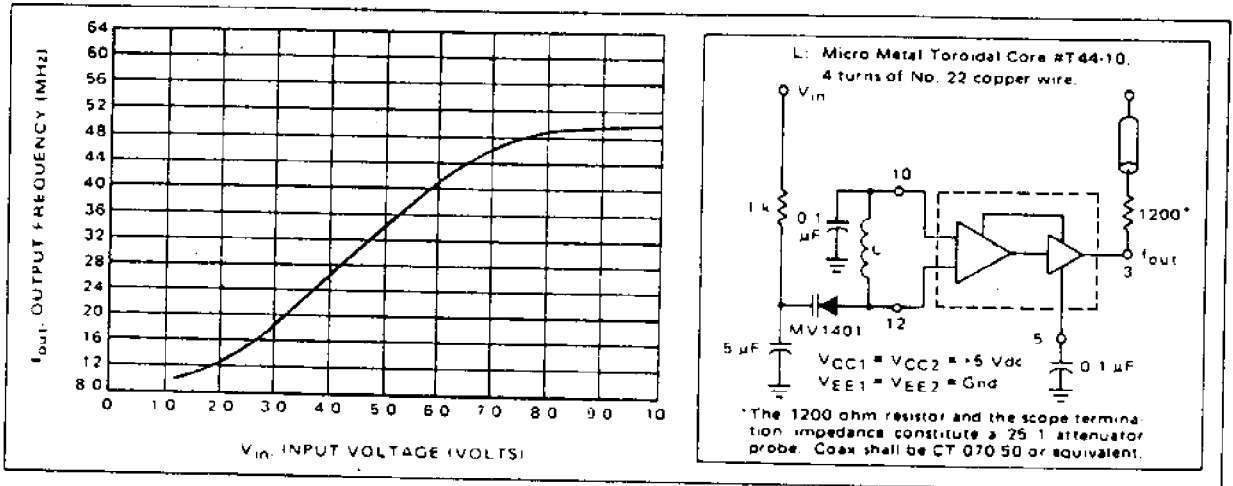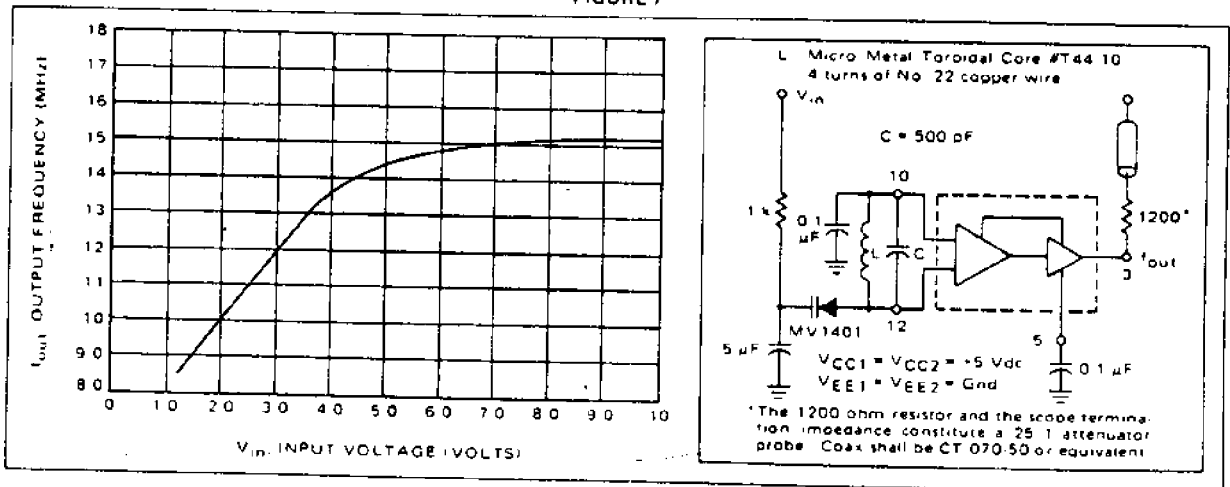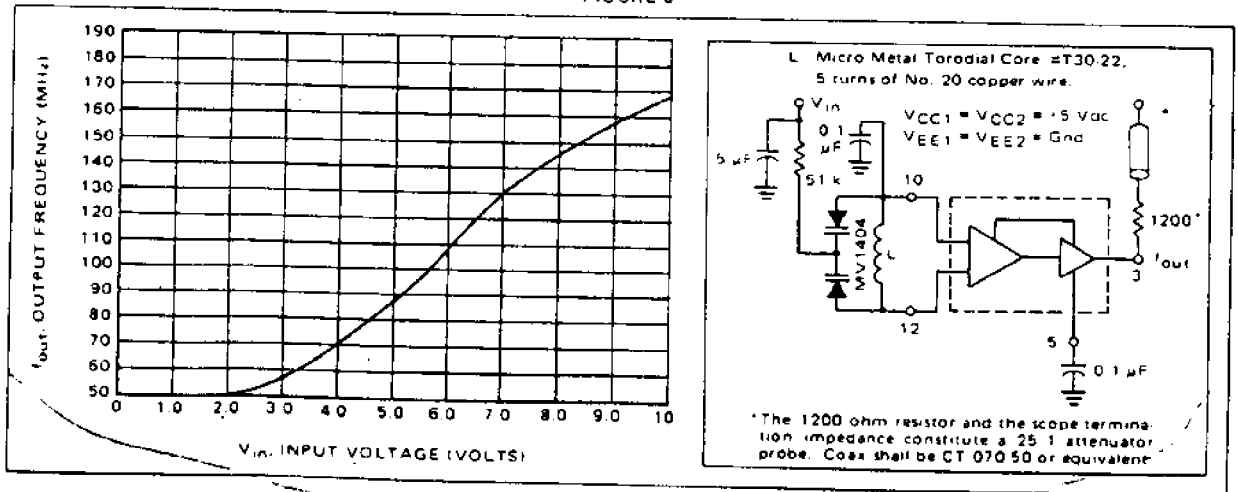The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching

(preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked loops and digital frequency synthesizers, see Motorola Application Notes AN-532A, AN-535, AN-553, AN-564 or AN594.

MC1648/MC1648M

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION
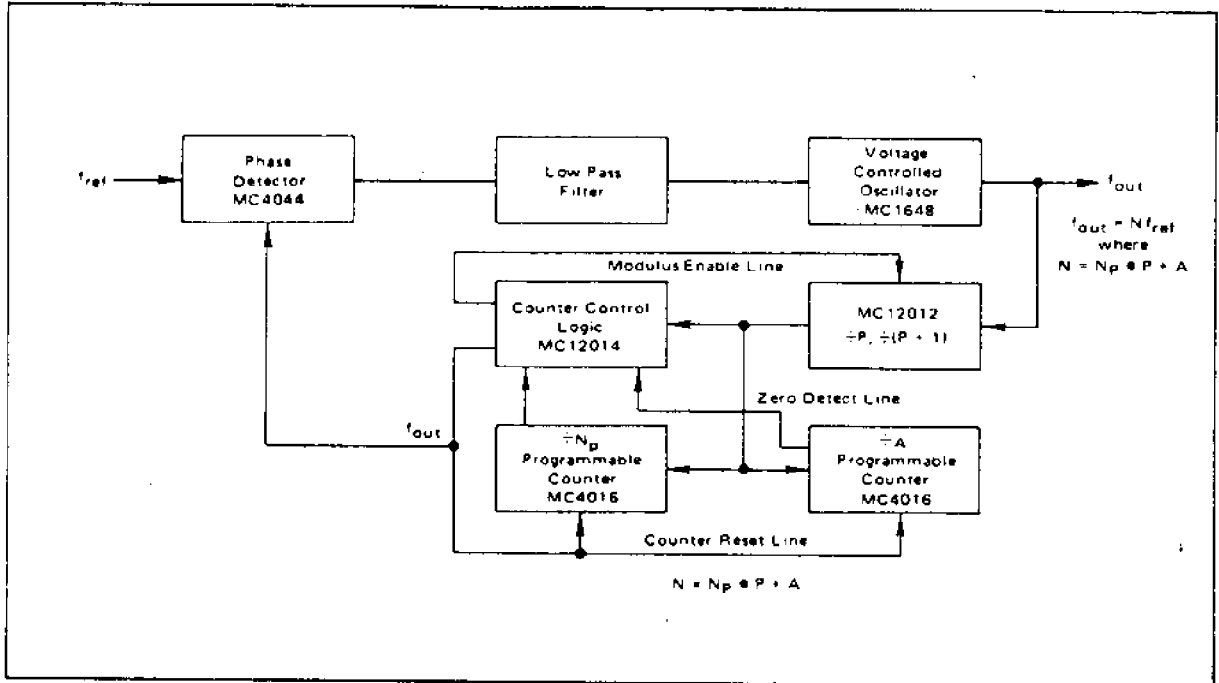
Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_EE.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT
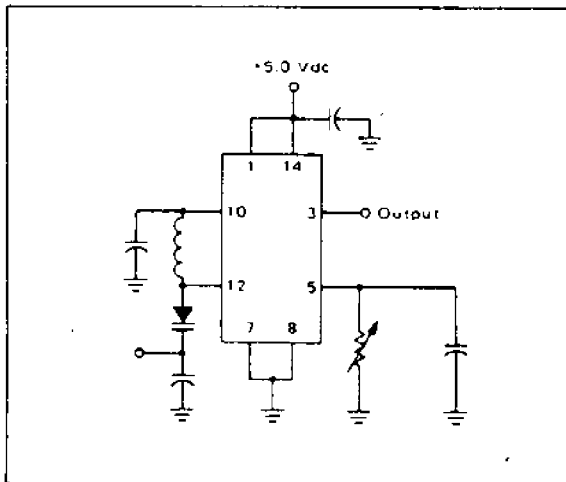
FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)
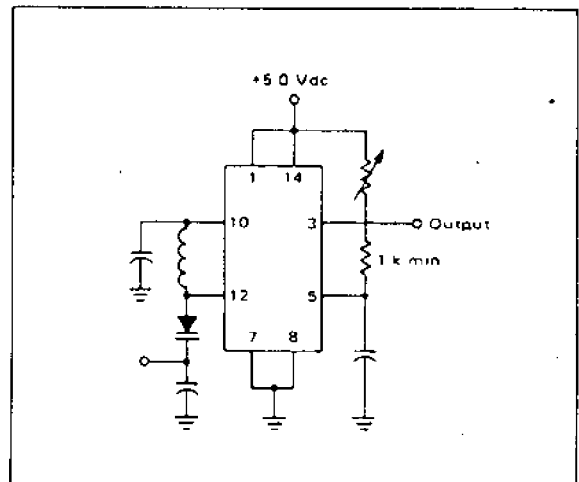
FIGURE 12 – CIRCUIT USED FOR
COLLECTOR OUTPUT OPERATION
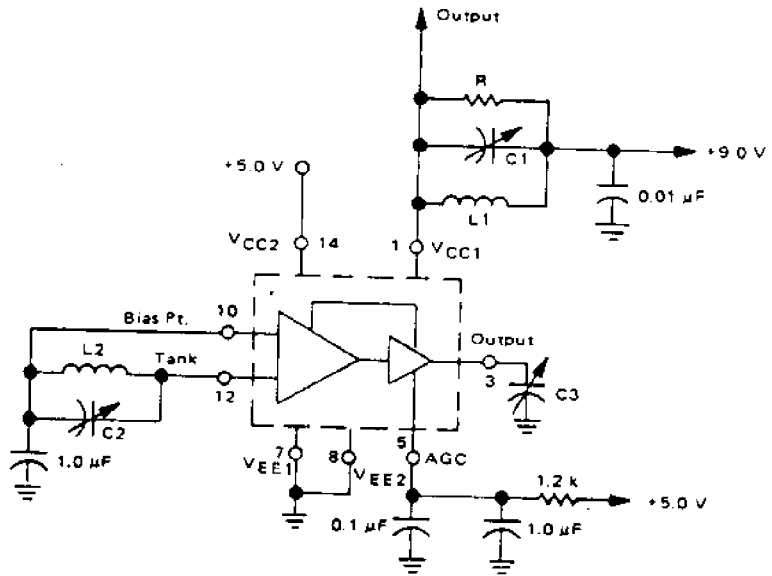
FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 100 MHz

C3 = 3.0 - 35 pF

Collector Tank

    L1 = 0.22 μH   C1 = 1.0 - 7.0 pF

    R = 50 Ω - 10 kΩ

    Rp of L1 and C1 = 11 kΩ @ 100 MHz Resonance

Oscillator Tank

    L2 = 4 turns #20 AWG 3/16" ID

    C2 = 1.0 - 7.0 pF
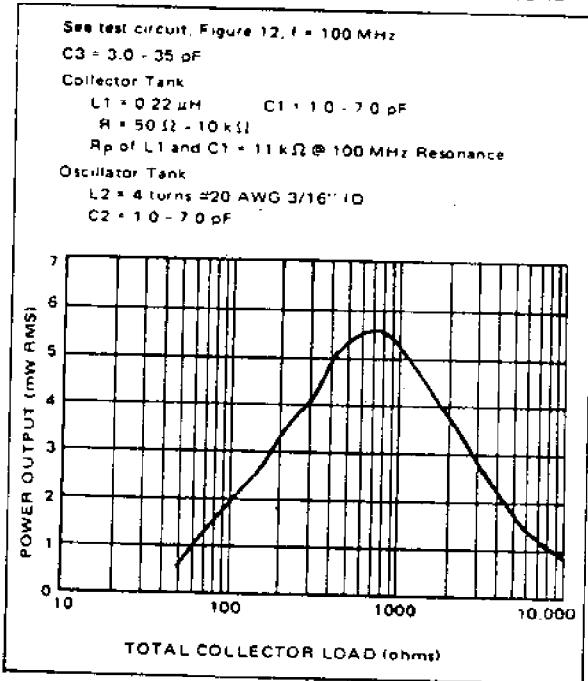
FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 10 MHz

C3 = 470 pF

Collector Tank

    L1 = 2.7 μH   C1 = 24 - 200 pF

    R = 50 Ω - 10 kΩ

    Rp of L1 and C1 = 6.8 kΩ @ 10 MHz Resonance

Oscillator Tank

    L2 = 2.7 μH

    C2 = 16 - 150 pF
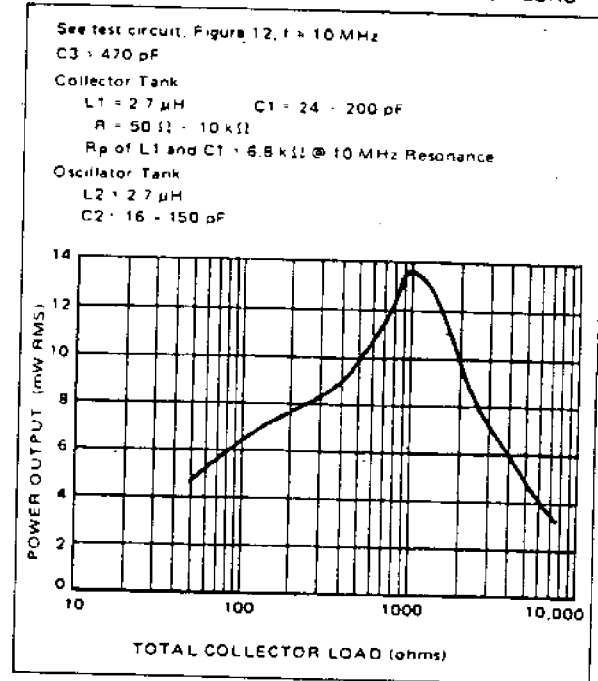
MC1690

UHF PRESCALER
TYPE D FLIP-FLOP
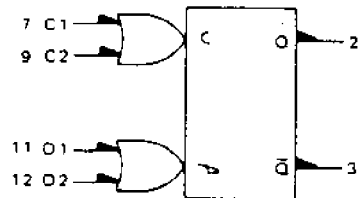
L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

C	D	Q_{n+1}
L	φ	Q_n
H	φ	Q_n
⌐	L	L
⌐	H	H

C = C1 + C2   φ = Don't Care
D = D1 + D2

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 200 mW typ/pkg (No Load)
f_{Tog} = 500 MHz min

Number at end of terminal denotes pin number for L package

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	59	—	—	mAdc
Input Current	I_{inH}							μAdc
Pins 7,9		—	—	—	250	—	—	
Pins 11,12		—	—	—	270	—	—	
Switching Times				Min	Typ	Max		ns
Propagation Delay	t_{pd}	—	—	—	1.5	—	—	—
Rise Time, Fall Time (10% to 90%)	t+, t−	—	—	—	1.3	—	—	—	ns
Setup Time	t_{setup}	—	—	—	0.3	—	—	—	ns
Hold Time	t_{hold}	—	—	—	0.3	—	—	—	
Toggle Frequency	f_{Tog}	500	—	500	540	—	500	—	MHz

4

FIGURE 1 — TOGGLE FREQUENCY TEST CIRCUIT
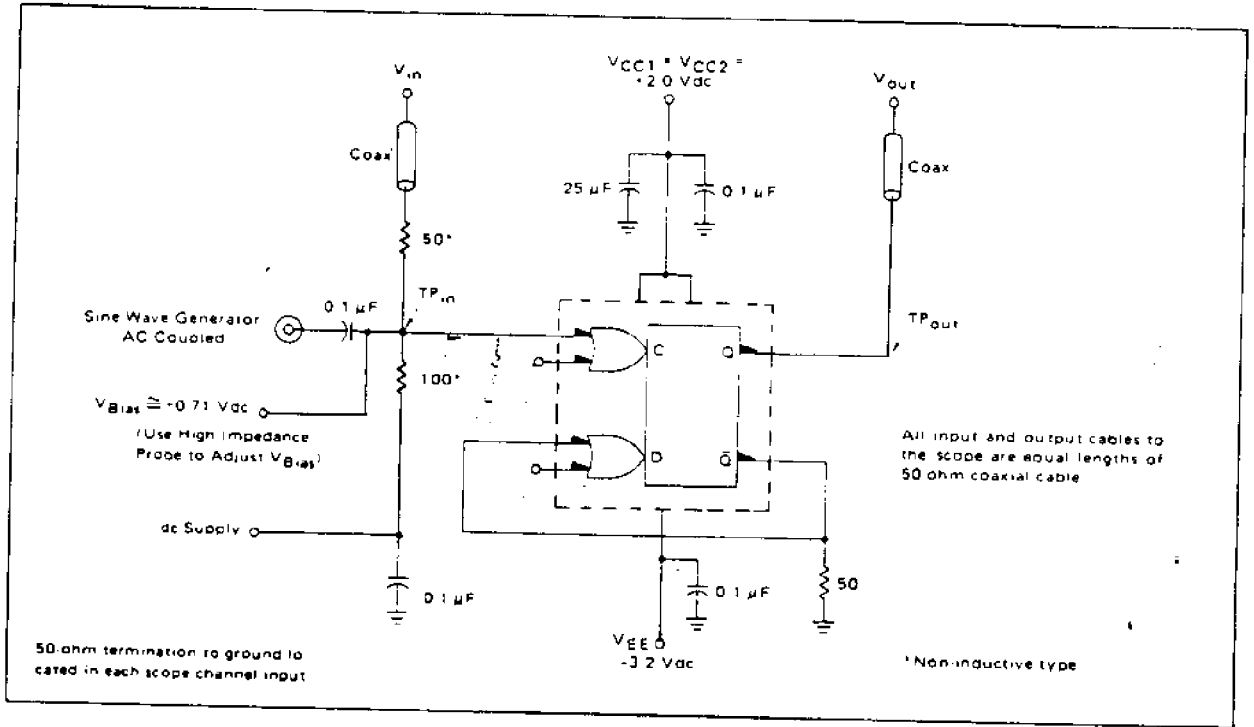
FIGURE 2 — TOGGLE FREQUENCY WAVEFORMS

The maximum toggle frequency of the MC1690 has been exceeded when either

1. The output peak to peak voltage swing falls below 600 millivolts.

OR

2. The device ceases to toggle (divide by two)
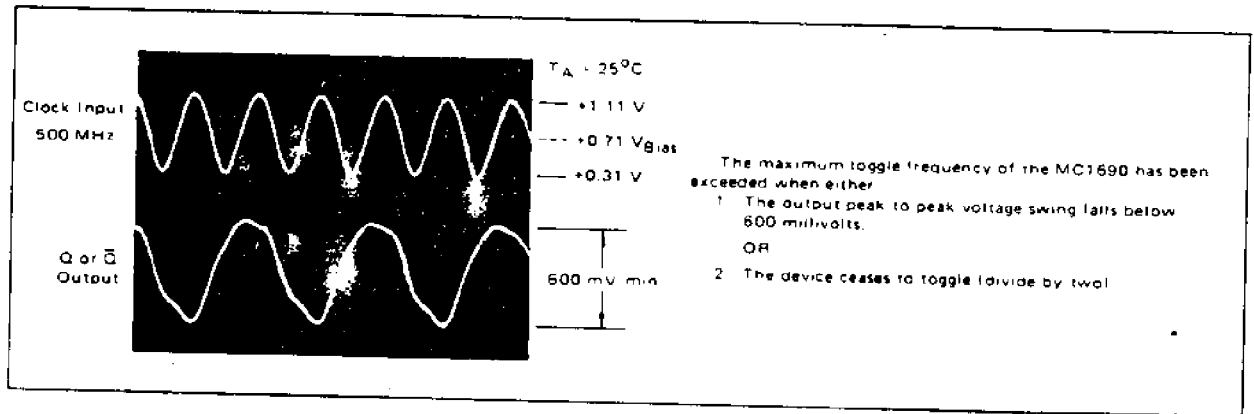
Note: All power supply and logic levels are shown shifted 2 volts positive.

MOTOROLA

Advance Information

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

The MC10H158 is a member of Motorola's new MECL family. The MC10H158 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 197 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

10KH

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 620

Quad 2-Input Multiplexer

V_{CC} = Pin 16
V_{EE} = Pin 8

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0-75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to 150 -55 to 165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ±5%)

Characteristic	Symbol	0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	Unit
Power Supply Current	I_E	—	53	—	48	—	53	mA
Input Current High Pin 9 Pins 3-6 and 10-13	I_{inH}	— —	475 515	— —	295 320	— —	295 320	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

		0° Min	0° Max	25° Min	25° Max	75° Min	75° Max	
Propagation Delay Data Select	t_{pd}	1.0 1.0	1.9 2.9	1.0 1.0	1.8 2.7	1.0 1.0	2.0 2.9	ns
Rise Time	t_r	0.7	2.2	0.7	2.0	0.7	2.2	ns
Fall Time	t_f	0.7	2.2	0.7	2.0	0.7	2.2	ns

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater then 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

Select	D0	D1	Q
L	✦	L	L
L	✦	H	H
H	L	✦	L
H	H	✦	H

✦ = Don't care

MOTOROLA

PHASE-FREQUENCY DETECTOR

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

Operating Frequency = 80 MHz typical

PHASE-FREQUENCY DETECTOR

P SUFFIX
PLASTIC PACKAGE
CASE 646
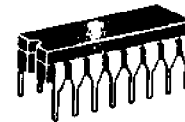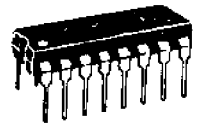
L SUFFIX
CERAMIC PACKAGE
CASE 632-02

LOGIC DIAGRAM
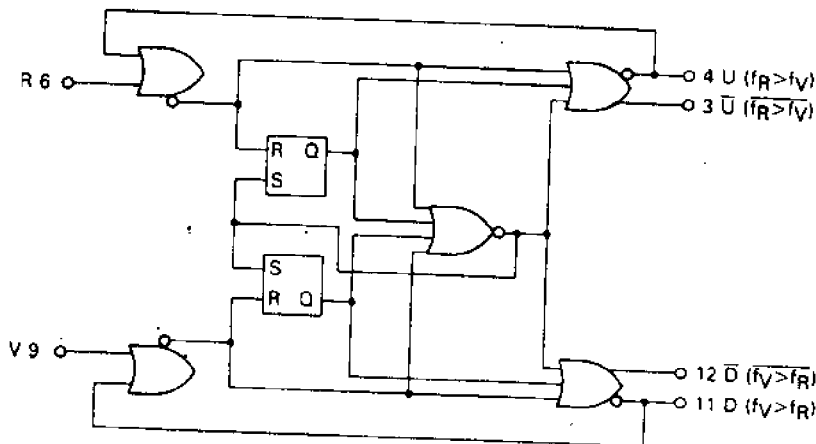
V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

INPUT		OUTPUT			
R	V	U	D	Ū	D̄
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0

X = Don't Care

PIN ASSIGNMENT

V_{CC1}	1	14	V_{CC2}
NC	2	13	NC
Ū	3	12	D̄
U	4	11	D
NC	5	10	NC
R	6	9	V
V_{EE}	7	8	NC
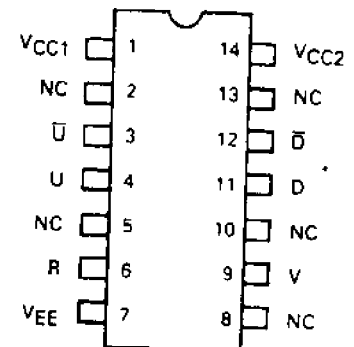
NC — No Connection

ELECTRICAL CHARACTERISTICS

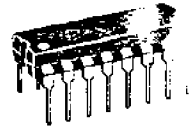The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to −2.0 V for −5.2 V tests.

Supply Voltage = −5.2V

													TEST VOLTAGE VALUES (Volts)				
										@ Test Temperature	$V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}		
										0°C	-0.840	-1.870	-1.145	-1.490	-5.2		
										25°C	-0.810	-1.850	-1.105	-1.475	-5.2		
										75°C	-0.720	-1.830	-1.045	-1.450	-5.2		

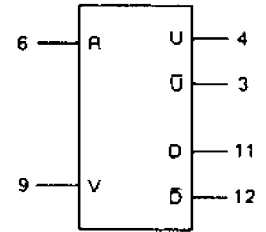| Characteristic	Symbol	Pin Under Test	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	$V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{EE}	(Vcc) Gnd
Power Supply Drain Current	I_E	7	-	-	-120	-60	-	-	mAdc	-	-	-	-	7	1,14
Input Current	I_{INH}	6	-	-	-	350	-	-	μAdc	6	-	-	-	7	1,14
		9	-	-	-	350	-	-	μAdc	9	-	-	-	7	1,14
Logic "1" Output Voltage	V_{OH}①	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	-	-	-	-	7	1,14
Logic "0" Output Voltage	V_{OL}①	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc	-	-	-	-	7	1,14
Logic "1" Threshold Voltage	V_{OHA}②	3 4 11 12	-1.020	-	-0.980	-	-0.920	-	Vdc		-	6,9		7	1,14
Logic "0" Threshold Voltage	V_{OLA}②	3 4 11 12	-	-1.615	-	-1.600	-	-1.575	Vdc		-	9 9 9 9	6 6 6 6	7	1,14

Supply Voltage = +5.0V

													TEST VOLTAGE VALUES (Volts)				
										@ Test Temperature	$V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{CC}		
										0°C	+4.160	+3.130	+3.855	+3.510	+5.0		
										25°C	+4.190	+3.150	+3.895	+3.525	+5.0		
										75°C	+4.280	+3.170	+3.955	+3.550	+5.0		

Characteristic	Symbol	Pin Under Test	0°C Min	0°C Max	25°C Min	25°C Max	75°C Min	75°C Max	Unit	$V_{IH\,max}$	$V_{IL\,min}$	$V_{IHA\,min}$	$V_{ILA\,max}$	V_{CC}	(VEE) Gnd
Power Supply Drain Current	I_E	7			-115	-60			mAdc					1,14	7
Input Current	I_{INH}	6				350			μAdc	6				1,14	7
		9				350			μAdc	9				1,14	7
Logic 1 Output Voltage	V_{OH}①	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
Logic "0" Output Voltage	V_{OL}①	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
Logic "1" Threshold Voltage	V_{OHA}②	3 4 11 12	3.980	-	4.020	-	4.060	-	Vdc			6,9		1,14	7
Logic "0" Threshold Voltage	V_{OLA}②	3 4 11 12	-	3.450	-	3.460	-	3.490	Vdc			9 9 9 9	6 6 6 6	1,14	7

## AC TESTS

PRF = 5.0 mHz
Duty Cycle = 50%
t+ = t− = 1.5 ns ± 0.2 ns
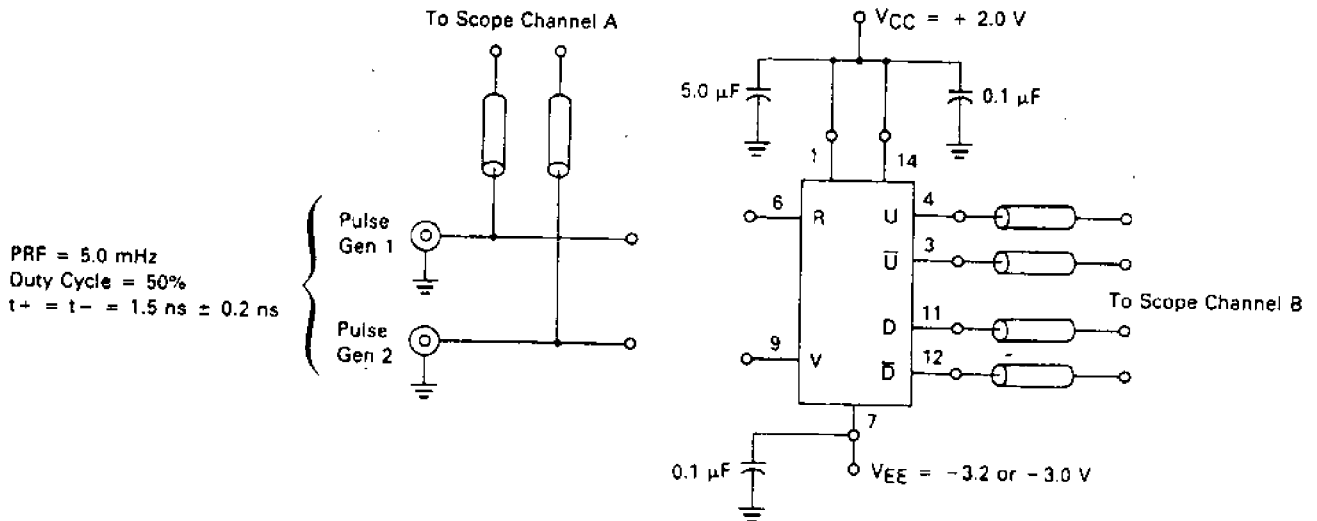
NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

2. Unused input and outputs are connected to a 50 Ω resistor to ground.

3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.
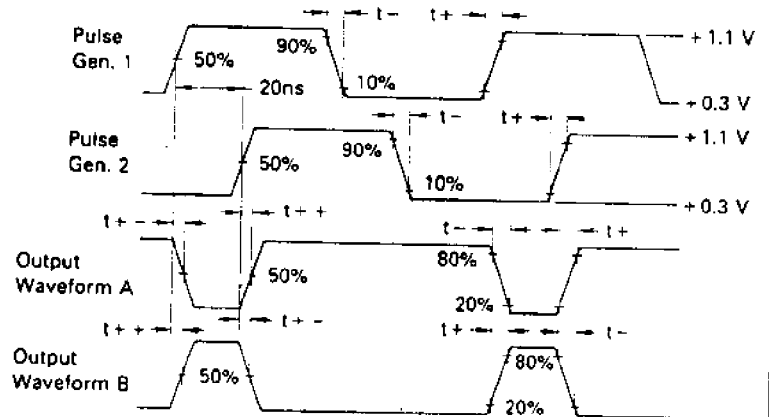
Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040			MC12540			Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW:			
				0°C	+25°C	+75°C	-55°C	+25°C	+125°C		Pulse Gen. 1	Pulse Gen. 2	V_EE -3.0 or -3.2 V	V_CC +2.0 V
				Max	Max	Max	Max	Max	Max					
Propagation Delay	t_{6+4+}	6,4	B	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6		
	t_{6+3-}	6,3	A	4.5	4.5	5.5	4.5	4.5	4.9		6	9		
	t_{6+11-}	6,11	B	6.4	6.4	7.7	6.4	6.4	7.0		9	6		
	t_{9+11+}	9,11	B	4.6	4.6	5.6	4.6	4.6	5.0		9	6		
	t_{9+3+}	9,3	A	6.0	6.0	7.2	6.0	6.0	6.6		6	9		
	t_{9+12-}	9,12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6		
	t_{9+4-}	9,4	B	6.4	6.4	7.7	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B								6	9		
	t_{11+}	11	B								9	6		
	t_{12+}	12	A								9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B								6	9		
	t_{11-}	11	B								9	6		
	t_{12-}	12	A								9	6		

7

APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.
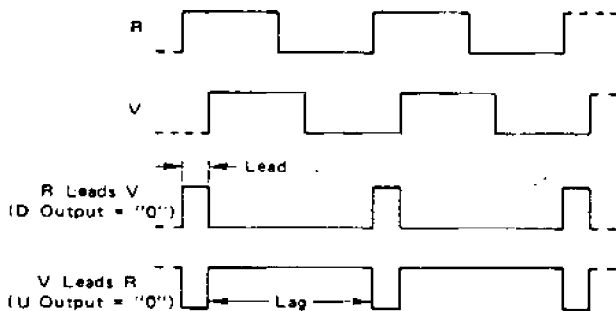
Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle — that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 — TIMING DIAGRAM

FIGURE 2 — TYPICAL FILTER AND SUMMING NETWORK

ANALOG DEVICES
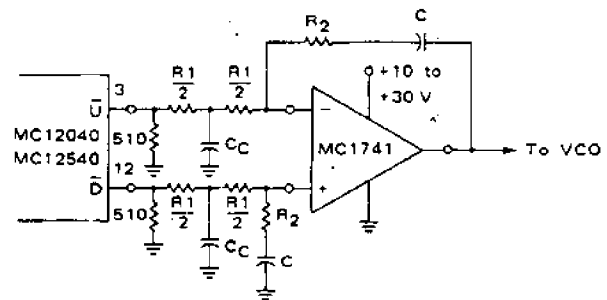
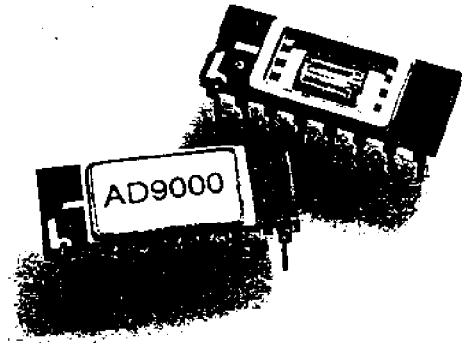# Ultra High-Speed 6-Bit Monolithic ADC

FEATURES
6-Bit, 75MHz Minimum Word Rates
No T/H Required
−55°C to +125°C Temperature
Overflow Bit for Cascading Units

APPLICATIONS
Image Processing
Video Digitizing
Radar Digitizing
Military Systems

GENERAL DESCRIPTION
The AD9000 A/D Converter is another addition to the expanding line of monolithic high-speed data converters available from Analog Devices. As model number AD9000SD, this 6-bit, 75MHz A/D can be operated over a temperature range extending from −55°C to +125°C, making it useful for a variety of applications in a wide diversity of environments. For applications requiring operation from 0 to +70°C, the AD9000JD is the recommended choice.

The AD9000 is a "flash" converter which uses 64 parallel comparators to digitize fast-moving analog input signals without the need for external track-and-hold (T/H) circuits. An overflow bit can be used for connecting multiple units in a cascade arrangement to obtain up to eight bits of digital data at MHz word rates.

Two cascaded devices can be used to obtain seven bits, and four units will provide eight bits of ECL-compatible output data.

Careful design techniques assure temperature coefficients which allow the unit to be operated over extended temperature ranges. The flexibility and usefulness of the AD9000 are also enhanced by its ability to operate with maximum positive and negative reference voltages applied simultaneously, as contrasted with other flash converters which often limit the user to a small range of voltage within the extremes.

All models of the AD9000 are packaged in standard ceramic DIP 16-pin configurations. Units processed to the requirements of MIL-STD-883, Method 5004, are also available for applications which require them.
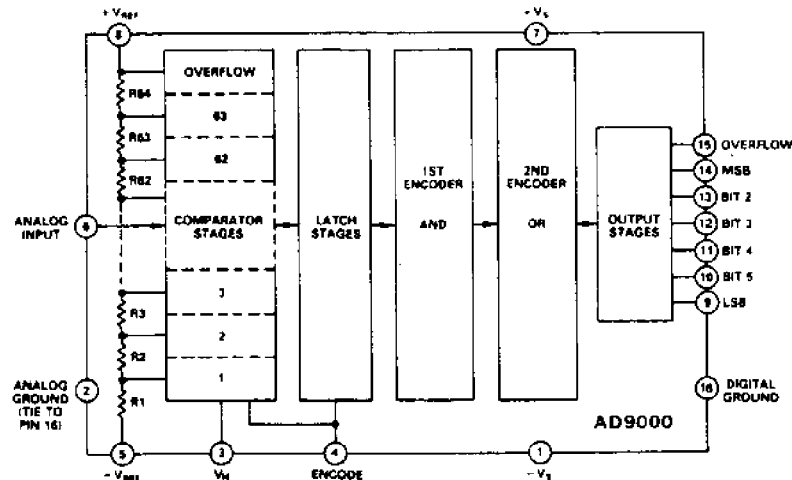
AD9000 Block Diagram

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Model Parameter	Units	AD9000SD[1] Min	Typ	Max	AD9000JD Min	Typ	Max
RESOLUTION (FS = Full Scale)	Bits		6			6	
LSB WEIGHT							
+V_REF = -V_REF = 0.512V	mV		16			16	
+V_REF = -V_REF = 1.024V	mV		32			32	
+V_REF = -V_REF = 2.048V	mV		64			64	
DC ACCURACY	%FS ±1 LSB		0.4			0.4	
Nonlinearity vs. Temperature	% of FS/°C		0.003			0.003	
Differential Linearity[2]							
+V_REF = -V_REF = 0.512V	LSB		0.75	1.0		0.75	
+V_REF = -V_REF = 1.024V	LSB		0.25	0.5		0.25	
+V_REF = -V_REF = 2.048V	LSB		0.2	0.4		0.2	
Integral Linearity[2]							
+V_REF = -V_REF = 0.512V	LSB		1.25	1.5		1.25	
+V_REF = -V_REF = 1.024V	LSB		0.7	1.0		0.7	
+V_REF = -V_REF = 2.048V	LSB		0.4	0.75		0.4	
Monotonicity		Guaranteed -55°C to +125°C			Guaranteed 0 to +70°C		
DYNAMIC CHARACTERISTICS							
In-Band Harmonics[3]							
dc to 1MHz							
+V_REF = -V_REF = 0.512V	dB below FS		44			44	
+V_REF = -V_REF = 1.024V	dB below FS		47			47	
+V_REF = -V_REF = 2.048V	dB below FS		47			47	
1MHz to 5MHz							
+V_REF = -V_REF = 0.512V	dB below FS		40			40	
+V_REF = -V_REF = 1.024V	dB below FS		40			40	
+V_REF = -V_REF = 2.048V	dB below FS		41			41	
5MHz to 8MHz							
+V_REF = -V_REF = 0.512V	dB below FS		30			30	
+V_REF = -V_REF = 1.024V	dB below FS		30			30	
+V_REF = -V_REF = 2.048V	dB below FS		31			31	
Conversion Time	ns		13			13	
Conversion Rate[4]	MHz	75	100		50		
Aperture Uncertainty (Jitter)	ps		25			25	
Aperture Time (Delay) (T_D)	ns		2			2	
Setup Time (t_s)[5]	ns	2			2		
Hold Time (t_H)[6]	ns	2			2		
Signal Transition Time[7]							
Input to Output Low (t_{pd} -)	ns	11	13	14	11	13	14
Input to Output High (t_{pd} +)	ns	8	10	12	8	10	12
Signal to Noise Ratio (SNR)[8]							
+V_REF = -V_REF = 0.512V	dB		36			36	
+V_REF = -V_REF = 1.024V	dB		37			37	
+V_REF = -V_REF = 2.048V	dB		36			36	
Signal to Noise Ratio (SNR)[9]							
+V_REF = -V_REF = 0.512V	dB		45			45	
+V_REF = -V_REF = 1.024V	dB		46			46	
+V_REF = -V_REF = 2.048V	dB		45			45	
Noise Power Ratio (NPR)[10]							
+V_REF = -V_REF = 0.512V	dB	27	29			29	
+V_REF = -V_REF = 1.024V	dB	27	29			29	
+V_REF = -V_REF = 2.048V	dB	27	29		27	29	
Transient Response[11]	ns			10			10
Overvoltage Recovery[12]	ns		5			5	
ANALOG INPUT (A_{IN})							
Voltage Range, Rated Performance	V	±0.5			±2		
Input Type		Unipolar (positive or negative) or Bipolar					
Input Current							
Hold (Latch) Mode	µA	-10			+10	-10	+10
Track (Sample) Mode[13]	µA		550	800		550	800
Input Capacitance[14]	pF		30			30	
Impedance[13]	kΩ		3.6			3.6	
Frequency Response[15] (75MHz Encode Rate)							
+V_REF = -V_REF = 0.512V	MHz		24			24	
+V_REF = -V_REF = 1.024V	MHz		20			20	
+V_REF = -V_REF = 2.048V	MHz		15			15	
REFERENCE INPUT							
Positive Reference (+V_REF)	V	-1.5		+2.0	-1.5		+2.0
Negative Reference (-V_REF)	V	-2.0		+1.5	-2.0		+1.5
Resistance	Ω	80	100	200	80	100	200
Bandwidth							
Small Signal, 3dB	MHz		25			25	
Large Signal, 3dB	MHz		20			20	

| Model Parameter	Units	AD9000SD[1] Min	Typ	Max	AD9000JD Min	Typ	Max
ENCODE COMMAND INPUT							
Logic Compatibility			ECL			ECL	
Digital "1" (Hold/Latch)	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0" (Track/Sample)	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Digital "1" Current	μA	5	15	35	5	15	35
Digital "0" Current	μA	5	15	35	5	15	35
Required Termination (to −2V)	Ω			50			50
Pulse Width							
Hold/Latch [t_{pw}(H)]	ns	5	7		5	7	
Track Sample [t_{pw}(T)]	ns	4	6		4	6	
Frequency[4]	MHz	75	100		50		
DIGITAL OUTPUT							
Format	Bits			6 Parallel (RZ) plus Overflow (NRZ)		
Logic Compatibility			ECL				
Digital "1"	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0"	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Required Termination (to −2V)	Ω	100			100		
Time Skew	ns			0.4			0.4
Coding			Binary (BIN)				
			Offset Binary (OBN)				
			No Data Ready Output Pulse				
POWER REQUIREMENTS							
+5V ±5% (+V_S)	mA		60	75		60	75
−5.2V ±5% (−V_S)	mA		67	85		67	85
Power Dissipation							
(+V_{REF} = −V_{REF} = 0V)	mW		650			650	
(+V_{REF} = −V_{REF} = 1V)	mW		690			690	
(+V_{REF} = −V_{REF} = 2V)	mW		810			810	
TEMPERATURE RANGE							
Operating (Case)	°C	−55		+125	0		+70
Storage	°C	−55		+150	−55		+150
THERMAL RESISTANCE[16]							
Junction to Air, θja (Free Air)	°C/W		95			95	
Junction to Case, θjc	°C/W		20			20	

NOTES

[1]Specifications for AD9000SD 883B same as AD9000SD.

[2]Encode Rate = 75MHz; Analog Input = 1kHz.

[3]Spurious in-band signals generated at 20MHz encode rate at analog inputs shown in .

[4]Some spec degradation may occur at word rates (encode frequencies) above minimum shown. See Figure 4 for typical relationship between analog input frequencies and encode rates.

[5]This is internal time set by design and is the minimum time before positive leading edge of Encode Command that a latch output must be at "1" for digital output to be generated by the latch.

[6]This is internal time set by design and is the minimum time after positive leading edge of Encode Command that a latch output must remain at "1" for digital output to be generated by the latch.

[7]Specifications with digital outputs terminated in 100Ω connected to −2V

[8]RMS signal to rms noise ratio with 500kHz analog input.

[9]Peak-to-peak signal to rms noise ratio with 500kHz analog input.

[10]DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz, and encode rate of 20MHz.

[11]For full-scale step input, 6-bit accuracy attained in specified time.

[12]Recovers to 6-bit accuracy in specified time after 150% FS input overvoltage.

[13]Measured in track/sample mode with A_{IN} = V_{REF}.

[14]Measured with A_{IN} = V_{REF}.

[15]Specified frequencies are maximums with no missing codes.

[16]Recommended maximum junction temperature is +150°C. When using ±2V references, this temperature may be exceeded unless some form of heat sinking and/or cooling air is used. Note θja specification.

Specifications subject to change without notice.

MECHANICAL DIMENSIONS

Dimensions shown in inches and (mm).
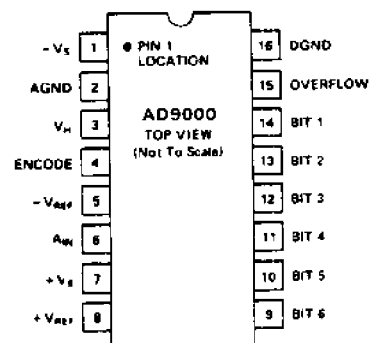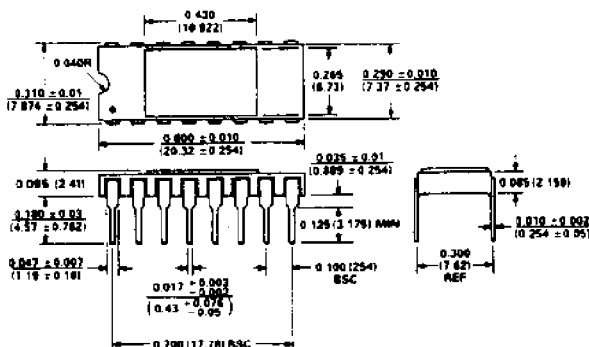
Outline & Pin Designations

ABSOLUTE MAXIMUM RATINGS

Parameter	Units	Lower Limit	Upper Limit
Supply Voltages			
+V$_S$	Volts	−0.3	+6.0
−V$_S$	Volts	−6.0	+0.3
Analog Input (A$_{IN}$)	Volts	−3.0	+3.0
Encode Command Input	Volts	−6.0	0.0
Reference Inputs			
+V$_{REF}$	Volts	−3.0	+3.0
−V$_{REF}$	Volts	−3.0	+3.0
Hysteresis Control Input	Volts	0	+3.0
Temperature			
Operating			
AD9000SD	°C	−55	+125
AD9000JD	°C	0	+70
Storage	°C	−55	+150
Lead Soldering (10 seconds)	°C		+300

PIN	SYMBOL	FUNCTION
1	−V$_S$	−5.2V NEGATIVE SUPPLY VOLTAGE
2	A$_{GND}$	ANALOG GROUND
3	V$_H$	HYSTERESIS CONTROL
4	ENCODE	ENCODE COMMAND INPUT
5	−V$_{REF}$	NEGATIVE VOLTAGE REFERENCE
6	A$_{IN}$	ANALOG INPUT
7	+V$_S$	+5V POSITIVE SUPPLY VOLTAGE
8	+V$_{REF}$	POSITIVE VOLTAGE REFERENCE
9	BIT 6	LEAST SIGNIFICANT BIT (LSB) OUTPUT
10	BIT 5	BIT 5 OUTPUT
11	BIT 4	BIT 4 OUTPUT
12	BIT 3	BIT 3 OUTPUT
13	BIT 2	BIT 2 OUTPUT
14	BIT 1	MOST SIGNIFICANT BIT (MSB) OUTPUT
15	OVERFLOW	OVERFLOW BIT OUTPUT
16	D$_{GND}$	DIGITAL GROUND

NOTE: A$_{GND}$ (PIN 2) and D$_{GND}$ (PIN 16) SHOULD BE CONNECTED TOGETHER AS CLOSE TO CASE AS POSSIBLE.

THEORY OF OPERATION

Refer to the Block Diagram of the AD9000.

Reference voltages (+V$_{REF}$ and −V$_{REF}$) applied across an array of identical resistors establish the analog operating span of the unit (+V$_{REF}$) − (−V$_{REF}$). The 64 resistors in the array divide the range into quantization levels equal to intervals of one least significant bit (LSB) between each resistor.

Each tap of the resistor array is connected to its associated voltage comparator input; the other input of each comparator is connected to the analog input (A$_{IN}$) signal. In this way, the comparator stages simultaneously compare the analog input with each one of the 64 (including OVERFLOW) quantization levels within the analog span set by the reference voltages.

Any comparator whose reference level is less than the analog input voltage will change its output state to a digital "1". Comparators whose reference levels are greater than the analog input will remain at digital "0".

Depending on the value of A$_{IN}$, anywhere from none to 64 comparators might have digital "1" at their outputs; the remaining comparators will be at digital "0". Obviously, processing that many bits of digital information is impractical if the data remain in this type of unwieldy format.

Wired-or logic circuits within the AD9000 re-encode the comparator outputs into a manageable, binary format of six bits of parallel data; along with an overflow bit which allows cascading units to obtain higher resolution.

The outputs of the comparators are applied to latches controlled by the ENCODE input. When the encode command is low (digital "0"), the latches are transparent; this is the track (sample) mode of the AD9000.

When the ENCODE input changes to high (digital "1"), the latches go into a "hold" (latch) condition, "freezing" the most recent digital outputs of the comparators and applying them to the encoding circuits.

The signal held in the latches is converted to binary form by the encoders and applied to the output stages as a six-bit digital representation of the analog signal which was present at the comparator inputs at the instant the ENCODE command made the change to the "hold" mode.

After 5–7 nanoseconds in the "hold" mode, the ENCODE input again transitions to a "track" condition; and the six bits of parallel data (but not the OVERFLOW output) return to zero (RZ). The "track" portion of the ENCODE command is 4–6 nanoseconds and during this interval the latches respond to the new state of the comparator outputs. The ENCODE signal then transitions again to the hold/latch (digital "1") mode and the cycle repeats. Track mode and hold mode intervals are dependent on duty cycle; times cited here are approximations for an encode frequency of 75MHz.

Time relationships of the hold/latch mode and track/sample mode of the ENCODE command are often influenced by the word rate selected by the user. At higher rates, it may be desirable to shorten the "hold" portion and lengthen the "track" portion; this technique can often enhance overall performance of the unit.

There is no need for an external track-and-hold circuit because the latches are performing the track/hold function. The aperture uncertainty (jitter) and aperture time (delay) specifications shown on the Specifications Table are "worst case" specs for the individual comparator cells, but are valid for the AD9000 because they manifest themselves as converter characteristics.

The good linearity tempco of the AD9000 is the result of using matched diffused resistors in the input network. Linearity in this type of converter is dependent primarily on the tracking of resistors; expressed in another way, resistance ratios are more important than absolute resistance values. Comparator thresholds in the AD9000 remain constant within a small fraction of 1LSB over the complete operating temperature range because of the close tracking of the resistors within the network. The temperature coefficients of comparator input bias currents and initial offset voltages which contribute to nonlinearity are kept small in the design of the AD9000 to minimize their effects.

Low offset voltages in the comparators are critically important for establishing the lower limit of the analog span set by the voltage references. When the reference voltage across the resistor chain decreases (the difference between $+V_{REF}$ and $-V_{REF}$ becomes less), the smaller value of the LSB approaches the value of the "worst case" comparator offset voltage. As the two get closer to one another, increasing linearity errors can restrict the lower limit of the analog span if comparator offset is relatively large.

The upper limit of the analog span is established by the common-mode range of the comparators because this range sets the maximum differential between $+V_{REF}$ and $-V_{REF}$. In this characteristic, too, the design of the AD9000 suggests its use instead of some competing devices.

Unlike some units, the AD9000 allows maximums of positive and negative reference voltages to be applied simultaneously. In some "flash" A/D's, the analog span is limited to some small range within the range of references, as opposed to being equal to the extremes. The ability of the AD9000 to operate with full-scale references improves its usefulness to the designer by imposing fewer constraints on operating conditions.

Like all flash converters, the input resistance of the AD9000 varies as a function of analog input voltage. This is because the individual comparators draw no current until the input voltage exceeds the reference voltage of the comparator; after that, the comparator's input current remains essentially constant. Consequently, the converter's input current and input resistance increase in a series of small steps as successive comparators are operated by an increasing analog input.

The input capacitance of the unit is the sum of the junction capacitances of the individual comparators. For many flash converters, this total is sometime sufficiently high to require a low-impedance driving source for the analog input. In the AD9000, however, input capacitance is typically 30pF, which is considerably lower than many competing devices and imposes fewer restrictions on the driving source.

AD9000 TIMING DIAGRAM
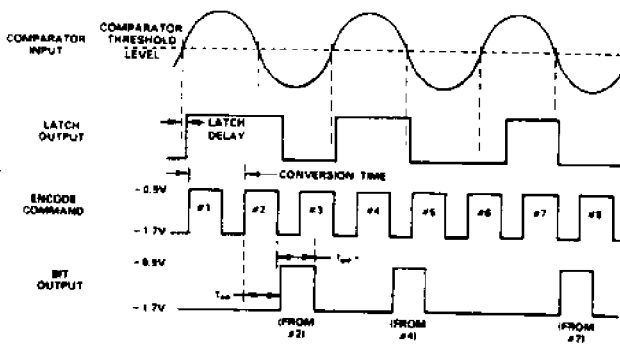Refer to Figure 1, AD9000 Timing Diagram.

Figure 1. AD9000 Timing Diagram

The comparator input shown on the top of the diagram is the analog input applied to one of the 63 comparators used to establish the digital value of the output word. The latch output is the latch associated with that comparator.

Each time the analog input applied to the comparator exceeds the reference level of the comparator, the corresponding latch output transitions to a digital "1" level.

When the encode command is at $-0.9V$ (digital "1") and the latch outut is at digital "1", a bit output associated with the comparator/latch combination will appear at the output. This statement is true only if:

A. The latch output is at digital "1" for a minimum of two nanoseconds before the positive-going leading edge of the encode signal (t_s).

B. The latch output remains at digital "1" for a minimum of two nanoseconds after the positive-going leading edge of the encode signal (t_h).

In Figure 1, there is no bit output associated with encode command #1 because the latch output was at the digital "1" level for less than the required two nanoseconds before the encode command changed. Encode command #2 however, combines with the same latch output to cause a bit output to appear.

At first glance, it might appear encode command #5 should combine with the second latch output to cause a bit output. It does not, however, because the latch output did not remain at a digital "1" level for a minimum two nanoseconds after the positive-going leading edge of the encode command.

Like t_s and t_h, the latch delay interval shown in Figure 1 is based on internal timing and is approximately one nanosecond long, but has only academic interest for the user. The important time intervals for proper use of the AD9000 are conversion time (typically 13ns); and signal transition time from the input to a positive output ($t_{pd}+$), and a negative output ($t_{pd}-$). Both signal transition times are typically 10ns.

In Figure 1, the widths of the digital "1" latch signals vary because of interaction with the hold commands. The first one is longer than normal because of encode pulse #2 causing the latch to continue to hold the "1" level. The second latch output is the expected width; while the third is shorter than normal because of encode pulse #6, which delays its transition by keeping it latched at digital "0".

APPLYING THE AD9000
The wired-or logic used in the AD9000 causes the data bits to go low (logic "0") whenever the OVERFLOW bit goes high. This characteristic allows two or more AD9000's to be operated in a cascaded arrangement when more than six bits of resolution are required.

When operating as a single 6-bit A/D, however, that feature of the AD9000 might be undesirable. This is because analog inputs greater than the positive reference voltage will appear as digital outputs of all "0", the same digital output expected of maximum negative inputs. The OVERFLOW bit can serve as a "flag" by going to digital "1" when the positive reference is exceeded.

For some applications, it may be preferable to have the logic output bits "lock up" at digital "1" for positive overvoltages; and digital "0" for negative overvoltages.

This can be accomplished with external logic, as shown in Figure 2, a typical connection for 6-bit operation of the AD9000.

A hex AND gate is used to bring the digital outputs high any time the OVERFLOW bit indicates the positive reference has been exceeded; this gate is wire-ored with the outputs of the AD9000.

Figure 2 contains other details on the preferred method for connecting the AD9000 into circuit applications. The suggested buffer amplifier for the analog input is the Analog Devices'
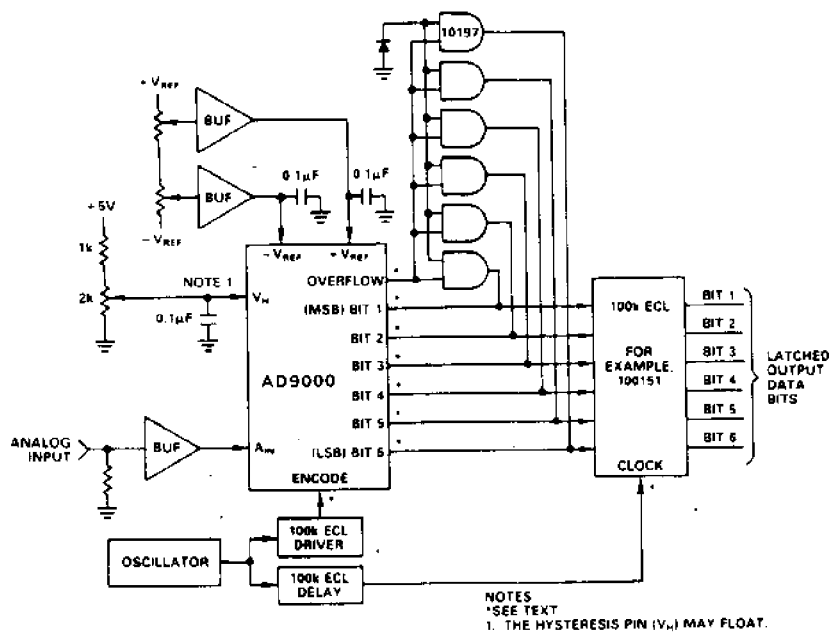
Figure 2. AD9000 6-Bit Operation

ADLH0033 or HOS-100; for the two reference voltages, AD741 devices are recommended. These high performance amplifiers are available in various models, making it easy for the user to select the unit best suited for his application.

The outputs of the reference buffer amplifiers are capacitively bypassed to help prevent noise from interfering with the performance of the AD9000. The ENCODE input is terminated in 50Ω connected to $-2V$; the CLOCK and digital outputs shown in Figure 2 are terminated in 100Ω, also to $-2V$.

If preferred, the hysteresis input (V_H) can be left floating, but experience indicates operation of the AD9000 may be improved with a variable voltage applied; this is particularly true at higher word rates.

Refer to Figure 3, which shows the effect of varying hysteresis control voltages.
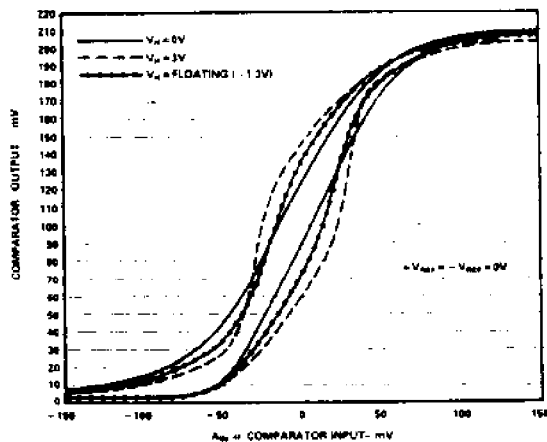

Figure 3. Comparator Output vs. Hysteresis Voltage

In this illustration of a typical comparator's output versus changes in hysteresis voltage, the combination of the two results in a "family" of classic hysteresis curves. The analog input (A_{IN}) voltage is measured in millivolts at the input of the comparator; the other comparator input, of course, is the voltage established by the tap on the resistor array discussed earlier. The comparator output shown on the vertical scale is internal to the AD9000 and appears at the output as an ECL-level signal.

For purposes of discussion of this particular comparator, $+V_{REF} = -V_{REF} = 0V$. Under these circumstances, the threshold of the illustrated comparator is close to 0mV. The thresholds of adjacent comparators would be at slightly different values, but the V_H hysteresis voltage would have the same general effect on the comparators' outputs.

Basically, the variations in hysteresis voltages change the gains of the comparators and slightly alter their outputs, as shown in Figure 3. In many applications, V_H could be left floating, which establishes a hysteresis voltage of approximately $+1.3V$. In other applications, however, the ability to introduce a small, predictable amount of hysteresis can enhance the AD9000's performance.

The hysteresis control input voltage can vary over a range of 0V to $+3.0V$, with voltages on the lower end of this span having only negligible effect. Variations between 0V and approximately $+0.5V$ cannot generally be detected as having an impact on the comparator gain.

The interaction between analog input frequencies and the encoding word rate is shown in Figure 4.
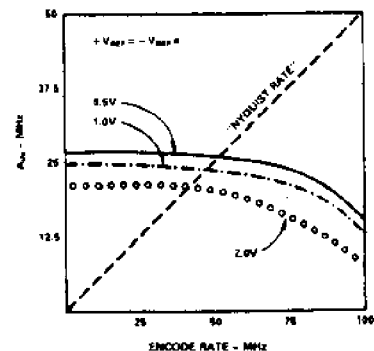

Figure 4. Analog Input vs. Encode Rate

The "Nyquist rate" is shown as a dotted line extending diagonally from dc to an analog input of 50MHz, and a word rate of 100MHz. As illustrated, the range of the analog input reference has a major effect on how closely the AD9000 approaches the Nyquist criteria.

In this figure, the analog input frequencies which are shown are the typical frequencies a user can expect to digitize without

missing codes. Note that as the "spread" of the reference voltages becomes larger, the expected analog input frequency becomes lower.

CASCADING AD9000's FOR MORE BITS
Earlier, there was an allusion to the capability for connecting multiple AD9000 units in a cascade arrangement to obtain more than six bits of digital information. Two cascaded devices would be used to obtain seven bits; and four cascaded devices used for

eight bits of output. Although it is theoretically possible to generate multiple bits by employing this method, the practical limitations involved in doubling the number of AD9000's for each additional bit tend to restrict the technique to a maximum of eight bits of digital data.

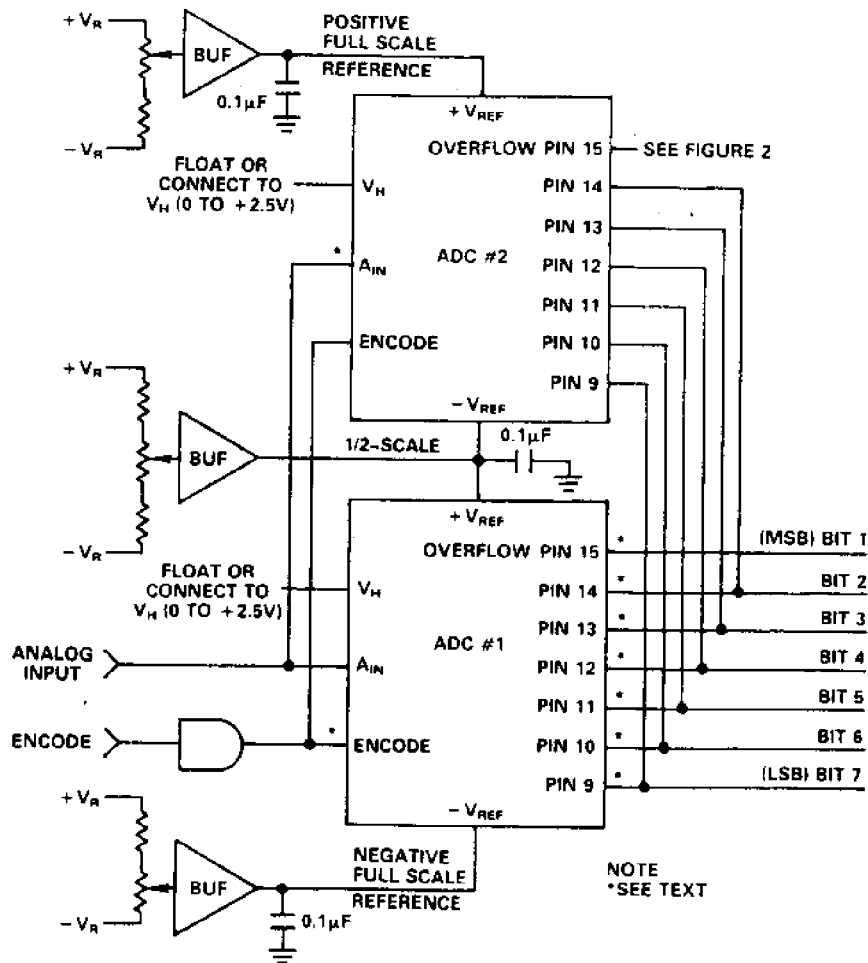A possible arrangement for achieving a 7-bit A/D converter is shown in Figure 5.

Figure 5. Cascaded AD9000's

When cascading units, the reference-resistor strings are connected in series and driven at the high, low, and mid-scale points. The 6-bit outputs of the two AD9000's are wired together and perform an *or* function; the Most Significant Bit (MSB) is provided by the OVERFLOW output of ADC #1.

If the analog input to the cascaded arrangement is below half-scale, the overflow bit of ADC #2 is low, and so are its output bits. This means the outputs of ADC #1 drive the output lines in response to the analog input.

When the analog input is above half-scale, the OVERFLOW bit of ADC #1 (the MSB) is high and acts as a carry; all the digital output bits of ADC #1 go low. ADC #2 converts the residual upper half-range, and its outputs drive the output lines. The conversions are occurring in parallel, so there is no loss of speed,

regardless of whether or not one or both of the cascaded A/D's are operating. The OVERFLOW bit of ADC #2 is wire-ored with external logic in a fashion similar to the method used when operating the AD9000 as a six-bit converter.

If this same technique is expanded to eight bits with four cascaded AD9000 devices, the analog reference span is divided into four equal parts; and a small amount of external logic is used to establish Bit 2 and minimize time skew. The need to double the divisions of the reference span with each succeeding bit is a major deterrent in extending this method beyond eight bits of resolution.

The loads used in cascade are the same as those with a single AD9000, i.e., the ENCODE input is terminated in 50Ω and the CLOCK and digital outputs are terminated in 100Ω, with all loads connected to $-2V$.

AD9000 EVAULUATION/TEST BOARD

Evaluating and/or testing the AD9000 A/D converter is made easier with the use of a printed circuit board which contains an A/D and the necessary test and reconstruction circuits.

A block diagram of this circuit is shown in Figure 6.

The AD9000 being evaluated or tested is connected in a back-to-back arrangement with a high-speed, high-resolution D/A converter. This combination allows the user to select a reconstructed version of the digitized analog input; or to examine the error signal when checking linearity. All necessary circuit components are contained on the 8.5" × 6.3" printed circuit board; the user needs to provide only power supply voltages.

Two models of boards are available, but the only difference between them is the model number of the A/D which is installed at the time of shipment. The AD9000JD/PCB includes a model AD9000JD unit; the AD9000SD/PCB has a model AD9000SD.

In both boards, the A/D converter is installed in a socket; and all other circuits are soldered into place. This technique allows

the evaluation board to be used as a test circuit for incoming AD9000 devices when production quantities are required. Complete operating instructions and a schematic are included with each board.

The test/evaluation board allows the user to check the performance of converters by providing a method for adjusting $+V_{REF}$, $-V_{REF}$, V_H, encode command pulse width, encode rate, and latch strobe delay. This kind of flexibility in assessing the unit's performance can supply valuable insight on how to obtain optimum performance from the AD9000 and get maximum benefit from its characteristics.

ORDERING INFORMATION

All versions of the AD9000 A/D converter are housed in 16-pin ceramic monolithic packages. Units operating over the standard temperature range of 0 to $+70°C$ are designated AD9000JD; for operation over an extended temperature range of $-55°C$ to $+125°C$, order model number AD9000SD. Devices which have been processed per MIL-STD-883, Method 5004, are available as AD9000SD/883B.

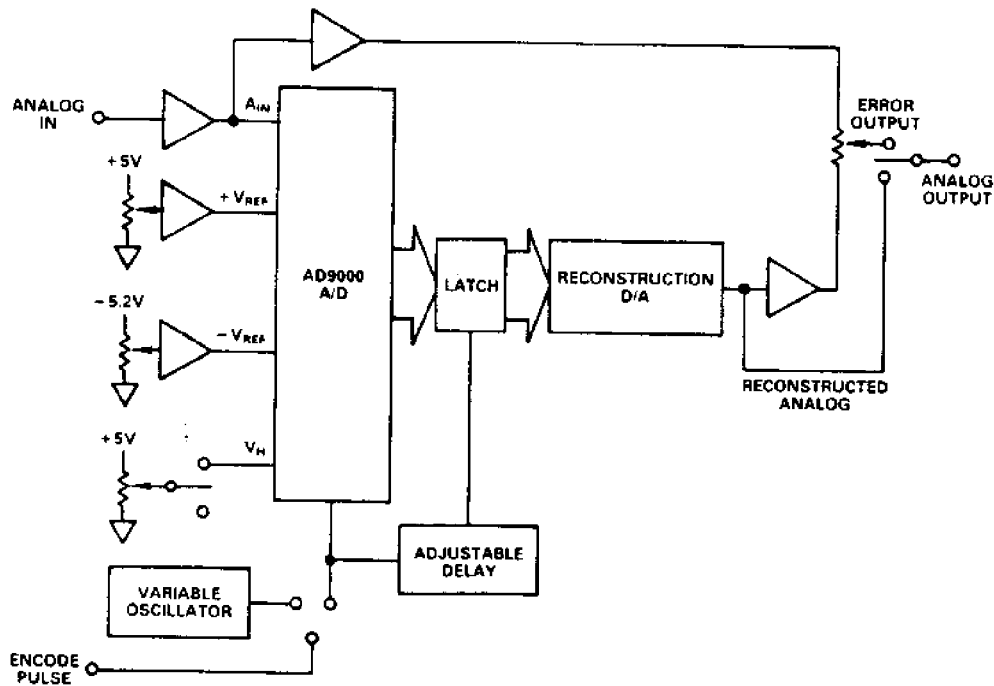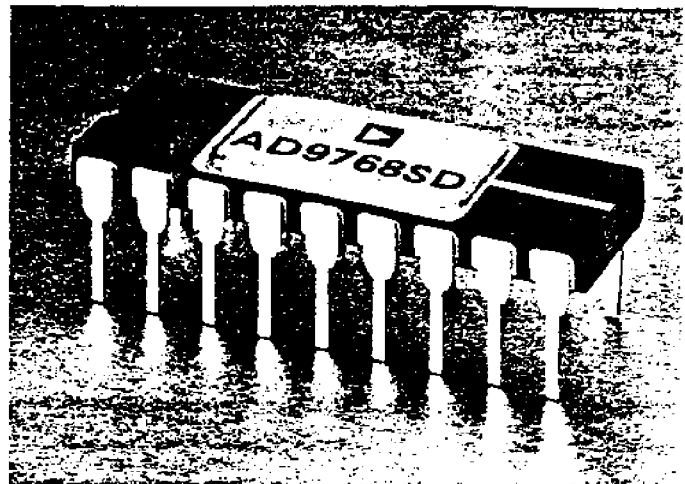Figure 6. AD9000/PCB Block Diagram

ANALOG DEVICES

Ultra High-Speed IC D/A Converter

AD9768

FEATURES
5ns Settling Time
100MHz Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High-Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MHz. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high-speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.
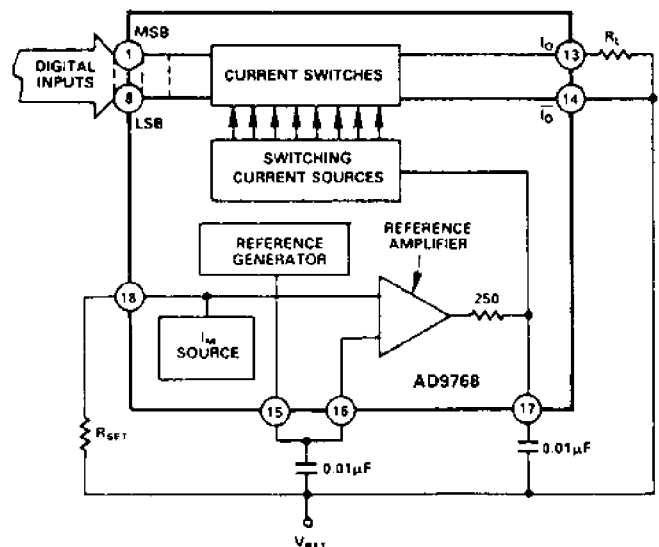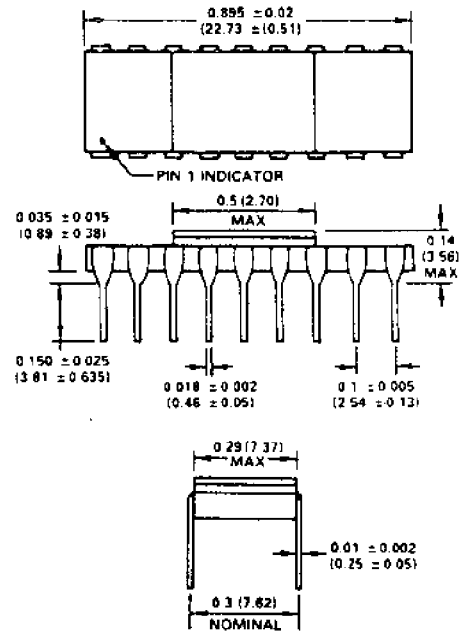
AD9768 Block Diagram (Conventional Operation)

SPECIFICATIONS
(typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; $R_L = 50\,\Omega$; $R_{SET} = 220\,\Omega$; $V_{RET} = 0V$)
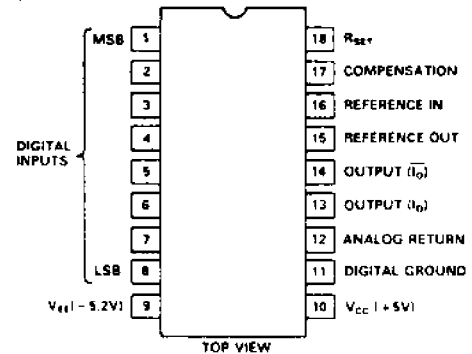
	Units	AD9768SD
RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	μA	78
ACCURACY[1]		
Differential Nonlinearity	± % FS	0.2
Integral Nonlinearity	± % FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	μA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	15
Reference Voltage (−1.26V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	−0.9
"0" =	V	−1.7
Coding	Binary (BIN) = Unipolar Out	
	Offset Binary (OBN) = Bipolar Out	
OUTPUT		
Current, Unipolar, FS	mA, max.	2 to 20 (30)
I_{OUT} ~ Pin 13		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
I_{OUT} ~ Pin 14		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V	−0.7 to +3.0
Impedance	Ω (±5%)	830
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/μs	400
Update Rate	MHz	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	−1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to −1.1 (−2)
Current-Multiplying Mode	mA (max)	0 to −5 (−7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	−0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8:	
	−0.1 V_M Input = 0mA I_{OUT}	
	−1.1 V_M Input = 0mA I_{OUT}	
	Measured at Pin 13; Digital "1" Applied to Bits 1-8:	
	−0.1 V_M Input = 1mA I_{OUT}	
	−1.1 V_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	kHz	250
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range at Pins 17 & 18	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8:	
	1mA I_M Input = 0mA I_{OUT}	
	5mA I_M Input = 0mA I_{OUT}	
	Measured at Pin 13; Digital "1" Applied to Bits 1-8:	
	1mA I_M Input = 4mA I_{OUT}	
	5mA I_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	MHz	40
POWER REQUIREMENTS		
−5.2V ±0.25	mA (max)	66 (70)
+5.0V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating	°C	−30 to +115
Storage	°C	−55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θja (free Air)	°C/W	90
Junction to Case, θjc	°C/W	20

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

AD9768SD PIN CONNECTIONS
(TOP VIEW)

|				
MSB	1		18	R_{SET}
	2		17	COMPENSATION
	3		16	REFERENCE IN
DIGITAL INPUTS	4		15	REFERENCE OUT
	5		14	OUTPUT (I_O)
	6		13	OUTPUT (I_O)
	7		12	ANALOG RETURN
LSB	8		11	DIGITAL GROUND
V_{EE} (−5.2V)	9		10	V_{CC} (+5V)

TOP VIEW

NOTES
[1] Relative to FS, including linearity (within voltage compliance limits).
[2] Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3] Applies when operating AD9768 as standard D/A.
[4] Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{REF} = 0V.
[5] 1% change in either power supply voltage causes 0.07% change in analog output.
[6] Case temperature.
[7] Maximum junction temperature 125°C.
Specifications subject to change without notice.

G-36
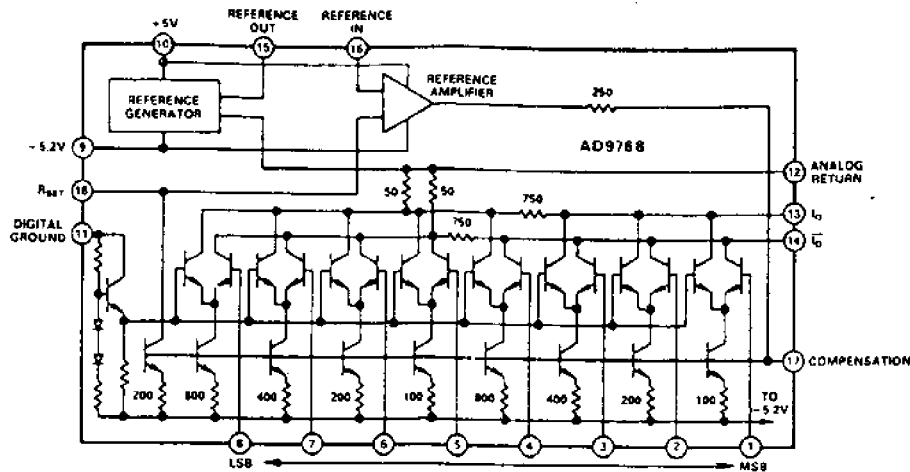
AD9768SD D/A Schematic

THEORY OF OPERATION
Refer to the AD9768SD schematic.

The transistors pictured on the bottom of the diagram, connected to paired transistors in the middle of the schematic, are current sources which are always "on". The paired transistors are differential current switches, designed to steer current from the current sources to either pin 13 (I_O) or pin 14 ($\overline{I_O}$).

Digital inputs applied to pins 1-8 determine which transistors will be operating in each pair and establish what current will flow at pins 13 and 14.

The transistor on the extreme left of the schematic is a base reference for the paired current switches and is used to assure the switches will be centered around an ECL voltage swing. The diodes connected to the base of this transistor are temperature compensation devices for the base-reference circuit.

There are three different current sources in the AD9768 D/A. The eight transistors shown on the bottom of the schematic are structured as two identical groups of four current sources, each of which is binarily weighted. The MSB group, comprised of the four on the right, is connected to the LSB group through a 15:1 current divider made up of two 50Ω and two 750Ω resistor networks. The geometry of the AD9768 guarantees the binary weighing ratios among the 100, 200, 400 and 800 resistors in each emitter circuit are correct.

The resistor values which are shown indicate the ratios among the resistors, and not their nominal values.

The third current source is a single transistor, pictured in the lower left portion of the schematic with its collector connected to pin 18 R_{SET}. Its function is to help establish the base voltage on the eight current sources; it works in conjunction with the external R_{SET} resistor selected by the user of the AD9768, and the reference amplifier. Current flowing through this transistor is referred to as I_M in the figures and test.

When the AD9768 is operating as a conventional current-output D/A converter, I_M develops a voltage across R_{SET} which is one of the inputs to the on-board reference amplifier shown in the schematic. The other input to this amplifier is the on-chip reference voltage of −1.26 volts.

The output of the reference amplifier adjusts the current-source base reference voltage at pin 17; this, in turn, adjusts the value of I_M in the single-transistor current source and causes it to develop a voltage across R_{SET} which maintains pin 18 at the

−1.26 volts of the on-chip reference supply.

To maintain good stability in the internal loop reference amplifier, a ceramic chip capacitor with a nominal value of 0.01μF should be connected to pin 17 COMPENSATION; minimum recommended value for this capacitor is 3900pF.

The temperature coefficient of the load resistor (R_L) can affect the performance of the AD9768 D/A converter, as it can with any current-output converter. The design and use of the AD9768 and its dependence on an external R_{SET} resistor, however, make it sensitive also to the tempco of R_{SET}. The user is cautioned to select R_L and R_{SET} resistors which have low temperature coefficients.

DIGITAL GROUND (pin 11) and ANALOG RETURN (pin 12) are normally connected together; this connection should be made as close as possible to the device case to minimize possible noise problems. The AD9768 D/A is similar to any other high-speed, high performance device: optimum use requires careful attention to all design details, including the layout of the circuit in which the converter is used.

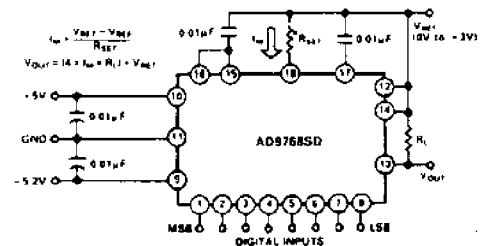## CONVENTIONAL AD9768
Refer to Figure 1, Conventional AD9768SD.

Figure 1. Conventional AD9768SD

The output current of the AD9768 appears at pin 13 (I_O) and develops a voltage across the load resistor R_L which is based on:

A. I_M (the current flowing through the single-transistor source discussed above)

B. Value of R_L.

I_M is a function of the return voltage (V_{RET}), the reference voltage (V_{REF}), and the value of R_{SET}; all of these are selected by the user for his application. The necessary equations for calculating precise values for each are part of Figure 1. As indicated,

the voltage drop across R_L is added to the return voltage; the resulting voltage is the total V_{OUT} of the converter.

VOLTAGE MULTIPLYING MODE

In addition to its use as an ultra-high speed current output D/A converter, the AD9768 can also be used as a two-quadrant multiplying D/A in either a voltage mode or a current mode.

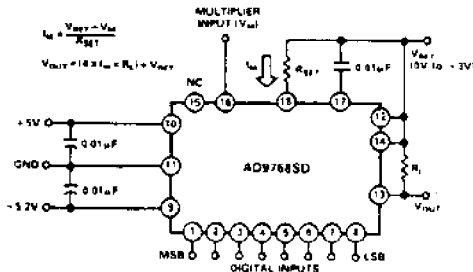Refer to Figure 2, Multiplying AD9768 (Voltage Mode).

Figure 2. Multiplying AD9768 (Voltage Mode)

When operating in this mode, the analog output of the AD9768 is influenced by the digital inputs and an external multiplying voltage (V_M) applied to pin 16 REFERENCE IN, which takes the place of the internal reference used when the D/A is operating in a conventional manner.

The value of I_M flowing through R_{SET} is set by the voltage of V_{REF} minus the multiplying voltage (V_M), divided by R_{SET}; the amount of this current is part of the equation which establishes the analog output (V_{OUT}) of the AD9768 and is chosen by the user for his application. As it is when operating the D/A in a conventional fashion, V_{REF} can be any value between 0 volts and +3 volts. V_M (for purposes of discussion here) is some negative voltage and can be varied over a range which is approximately 1 volt peak-to-peak.

If the load resistor (R_L) has a value of 50 ohms, if R_{SET} has a value of 220 ohms, and if V_{REF} is 0V, the center of the V_M voltage will be $-0.6V$; and it can vary from $-0.1V$ to $-1.1V$. Typically, the frequency of these variations has an upper limit of 250kHz when operating in the voltage multiplying mode; that frequency is the 3dB point of the bandwidth of the internal reference amplifier.
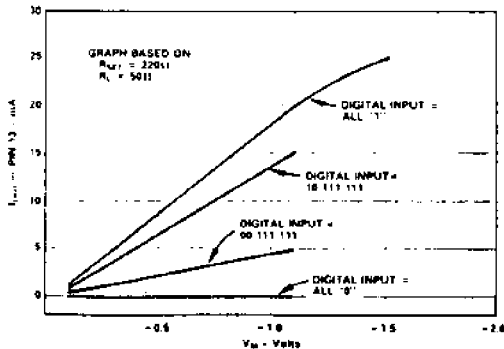
Figure 3. I_{OUT} vs. Multiplying Voltage

The combined effects of variations in V_M and changes in digital input values are shown in Figure 3, I_{OUT} vs. Multiplying Voltage. In this illustration, the ordinate of the graph is expressed in terms of milliamps of I_{OUT} current at pin 13. V_{OUT}, of course, will be a function of the value of R_L chosen by the user.

The negative value of V_M on the horizontal axis is shown starting at approximately $-0.1V$, rather than 0V, because the AD9768 must have some small value of voltage applied to perform a multiplying function. For the conditions shown in the figure, output current starts to become nonlinear at approximately

20mA because of the maximum 30mA output drive capabilities of the device. Different values for R_{SET} and R_L would alter the point where limiting first appears.

CURRENT MULTIPLYING MODE

The AD9768 D/A converter can be operated at markedly higher multiplying rates when operated in a current-multiplying mode, as contrasted with the voltage-multiplying mode. Refer to Figure 4, Multiplying AD9768SD (Current Mode).
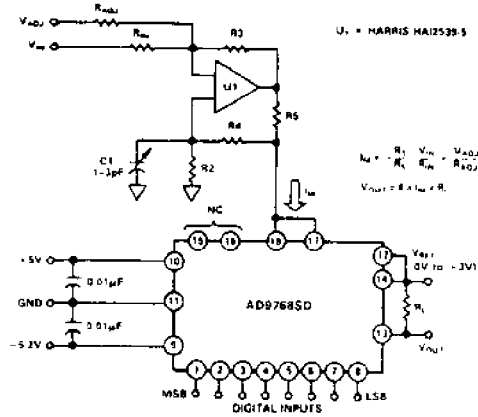
Figure 4. Multiplying AD9768SD (Current Mode)

In this mode, the internal reference amplifier and its inherent frequency limitations are replaced by a current source comprised of U1 and associated circuits. These circuits supply a unipolar current I_M which is one-fourth the full-scale output current (with digital "1" applied to all inputs) and set current flow through the load resistor.

V_{IN} is some voltage chosen by the user for his particular application; the value of this voltage is based in part on the size of the load resistor and the 0mA to 5mA range of I_M. V_{IN} can have frequency components as high as 40MHz. V_{ADJ} and R_{ADJ} provide an offset adjustment to compensate for the dc component of V_{IN} to assure I_M is always a unipolar current between 0mA and 5mA. The values of the required voltages and resistors can be calculated using the equations which are part of Figure 4.

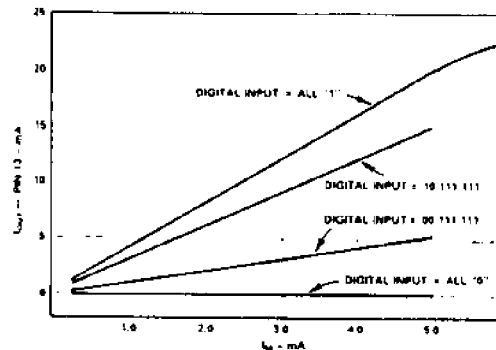Refer to Figure 5, I_{OUT} vs. Multiplying Current.

Figure 5. I_{OUT} vs. Multiplying Current

As shown, I_M can vary over the range of 0mA to 5mA; a value of approximately 0.3mA may be the practical lower limit because of nonlinearities at extremely small current levels. These changes in I_M are combined with variations in digital inputs, producing complex changes in the output current (at pin 13) and in V_{OUT}. The "rounding" of the current curve in the graph is the result of I_{OUT} approaching the 30mA maximum drive capabilities of the AD9768 and needs to be taken into account to assure optimum performance in the selected application.

Appendix H

End Notes and References

ENDNOTES

[1] Stewart, William K. 1985. "Advanced Observation Inspection ROV for 6,000 Meter Operations."

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[3] Cherin, Allen H. 1983. An Introduction to Optical Fibers.

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