DAA Technical Memorandum ERL ARL-115

ON EXPANDING (REMOTE) CONTROL CAPABILITY BY DIGITALLY SELECTING MATRIX ELEMENTS

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noaa NATIONAL OCEANIC AND ATMOSPHERIC ADMINISTRATION / Environmental Research Laboratories

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ILLUSTRATIONS

ON EXPANDING (REMOTE) CONTROL CAPABILITY BY DIGITALLY SELECTING MATRIX ELEMENTS

Robert H. Cordella, Jr.

Abstract. This document explains a method of expanding the number of command closures available from any system; but, it has particular benefit in remote control applications. The explanation begins with the theory of operation (algorithm) and proceeds through levels of increasing completeness to as-built schematics, layouts, and parts lists.

1. INTRODUCTION

Performing experiments remotely located from the investigator or operator necessitates sending certain instructions or indicators to control the equipment. These signals are commonly called commands in the scientific balloon community or flags in the computer community. In the former, where the experiment is probably 20 miles overhead and could be hundreds of miles removed laterally, such commands are issued via radio channels. Usually, they result in relay closures to activate equipment or parts thereof. This paper discusses a method of increasing the number of independent closures without changing the coding between the transmitter and receiver, or the output of the receiver.

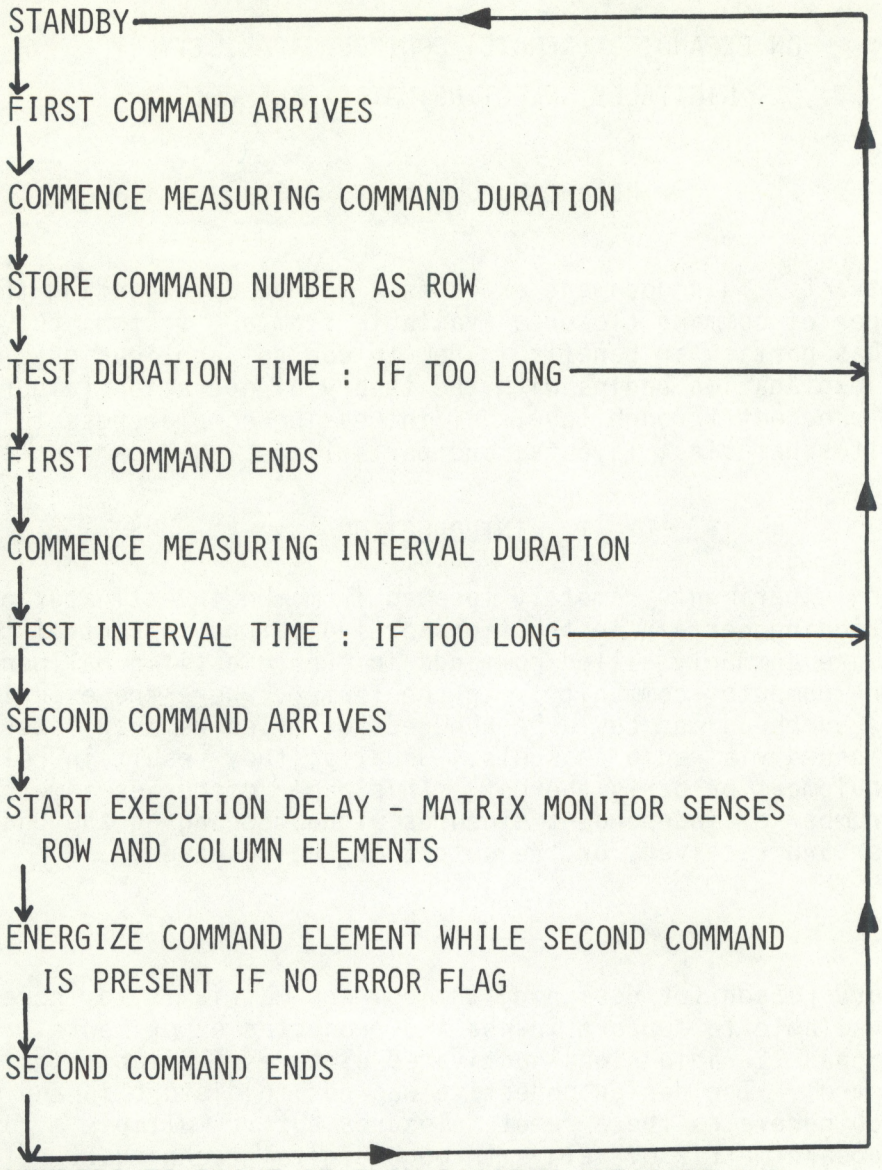
2. PURPOSE

The primary reason for designing the command matrix is to increase the number of closures available to support in-use and projected experiments. The balloon-borne receiver has 12 radio signal activated closures available for balloon and experiment control. The design objective was not to disturb in any way the equipment which generated these remote closures but to multiply a portion of them by driving a square matrix of relays through digital techniques.

3. THE ALGORITHM

In this design, sequential digital techniques enable two of N commands: C_1 through C_n applied sequentially to select a certain element: C_i, C_j in a two-dimensional square matrix. Also, certain safety features are included to facilitate the interface of machine and operator. The safety features include: 1) certain minimum or maximum time constraints; 2) feedback to prevent multiple matrix element (relay) activation; and 3) an error flag indicating multiple commands to the output matrix.

Figure 1 describes the algorithm's flow and Figure 2 depicts its timing. (Positive logic convention is used throughout the discussion and in drawings where possible.) Prior to the arrival of a command the machine is in a standby mode: state Ø. The arrival of command C_i causes the logic to enter state 1 during which it stores the command number and self checks to be certain that



NUMBERS TO RIGHT OF FLOW DIAGRAM INDICATE THE MACHINE'S CORRECT STATE.

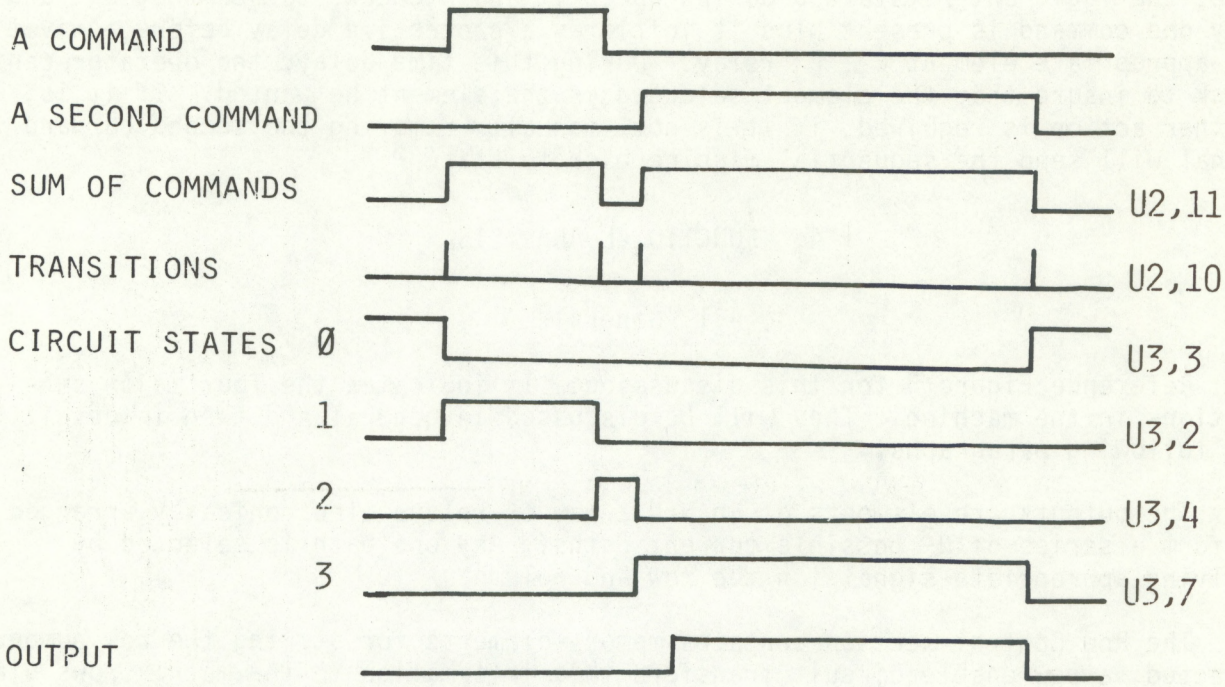
META-ALGORITHM

A. PRESENCE OF A COMMAND IMPLIES AN ODD STATE NUMBER AND VICE VERSA.

B. PRESENCE OF A COMMAND IMPLIES AN EVEN STATE NUMBER AND VICE VERSA.

C. IF A. OR B. TEST FALSE, RESET MACHINE.

Figure 1. Algorithm (ARL-0012).



TIME SCALE ⟶ ⟵ 10 SEC

TIMES CHECKED OR FORCED BY CIRCUIT

A. STATE 1, 1.25 SEC MIN

B. STATE 2, 20 SEC MAX

C. OUTPUT DELAYED 10 SEC FROM STATE 3 TO ALLOW OPERATOR TO CONFIRM ROW AND COLUMN PRIOR TO ACTIVATION.

Figure 2. Timing Waveforms.

one and only one command is present. Removing the first command places the machine in state 2 during which time between commands is measured. If the second command fails to arrive within the prescribed time, the circuit resets the logic to its standby mode: state Ø. If the second command C_j arrives within the appropriate time, the logic enters state 3 during which it again checks to see that one and only one command is present plus it initiates a protective delay before activating the appropriate element C_i, C_j relay. During this time delay, the operator can check to insure that the element selected is the element he wanted. If it is, no further action is required, if it is not, manually removing the second command signal will send the sequential machine back to state Ø.

4. FUNCTIONAL ANALYSIS

4.1 General

Reference Figure 3 for this discussion. It indicates the four major subsections in the machine. They will be discussed in general and then in detail in the following paragraphs.

The outputs are elements of an NxN array of relays electronically arranged to form a series of N^2 possible current paths. Any one path is selected by applying appropriate signals on the row and column.

The Row Control section contains memory elements for storing the row number selected; a row enable circuit transfers this information to the matrix rows via current drivers for each row.

The "State" control section orchestrates the entire operation. It receives all the command inputs from the receiver, detects their beginning and end points, and keeps track of the circuit's condition during the two command sequence. Control logic supplies the necessary timing and safety interlocks to produce a sequential machine.

The Matrix Monitor converts the row and column information to two binary words and an error flag for transmission to the operator.

4.2 Output Matrix

The matrix is best described by referring to Figure A7. It is shown as a 49 element array but it need not have all the elements (relays) in place or it could be expanded to have more elements. In either case each element is a unidirectional current path selected by activating one row and one column. Since each path is polarized, row drivers supply a positive voltage and column drivers supply a path to ground. Since the command receiver supplies closures to ground, they are used directly on the appropriate columns. This eliminates: 1) a controlled current sink; and 2) remembering what column was selected if the column command is given second.

4.3 Row Control

This circuit with its input and output connections is depicted in Figure 4. Prior to receiving a command, inputs "B", "1", and "3" are all logic zero; input

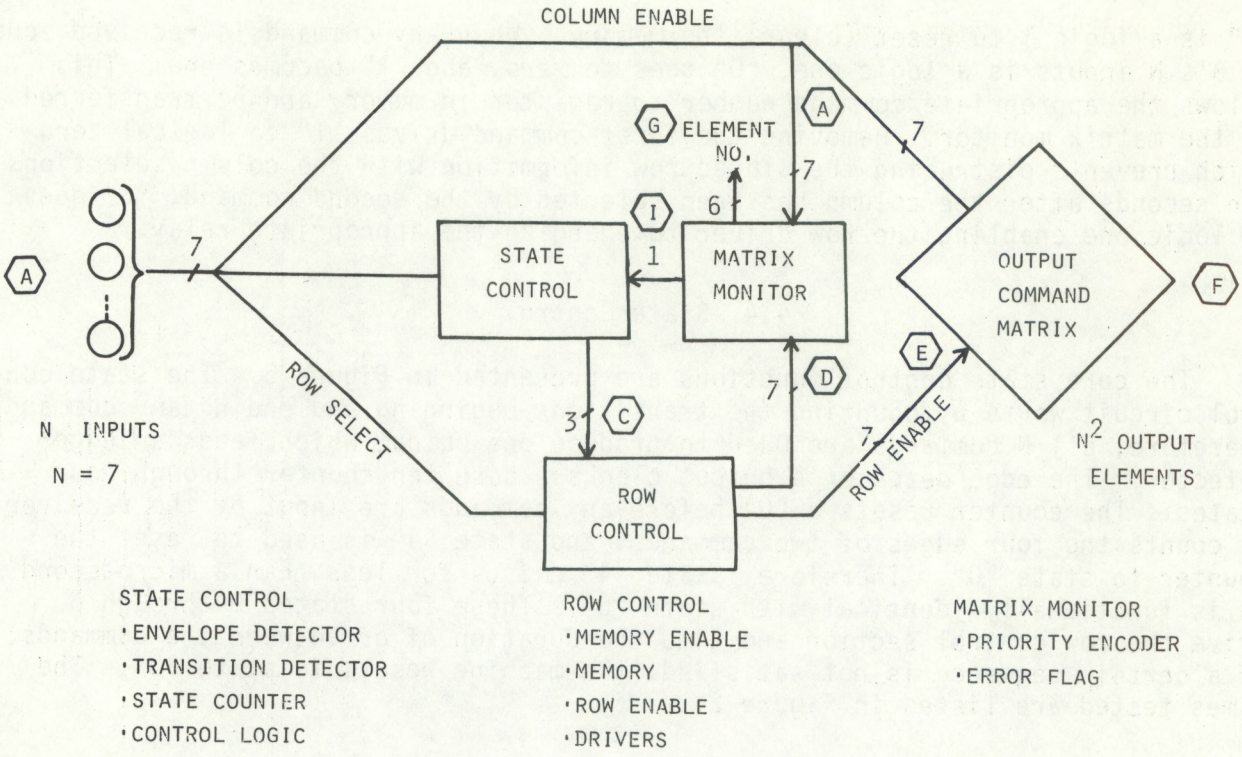


Figure 3. Function Diagram (ARL-0011).

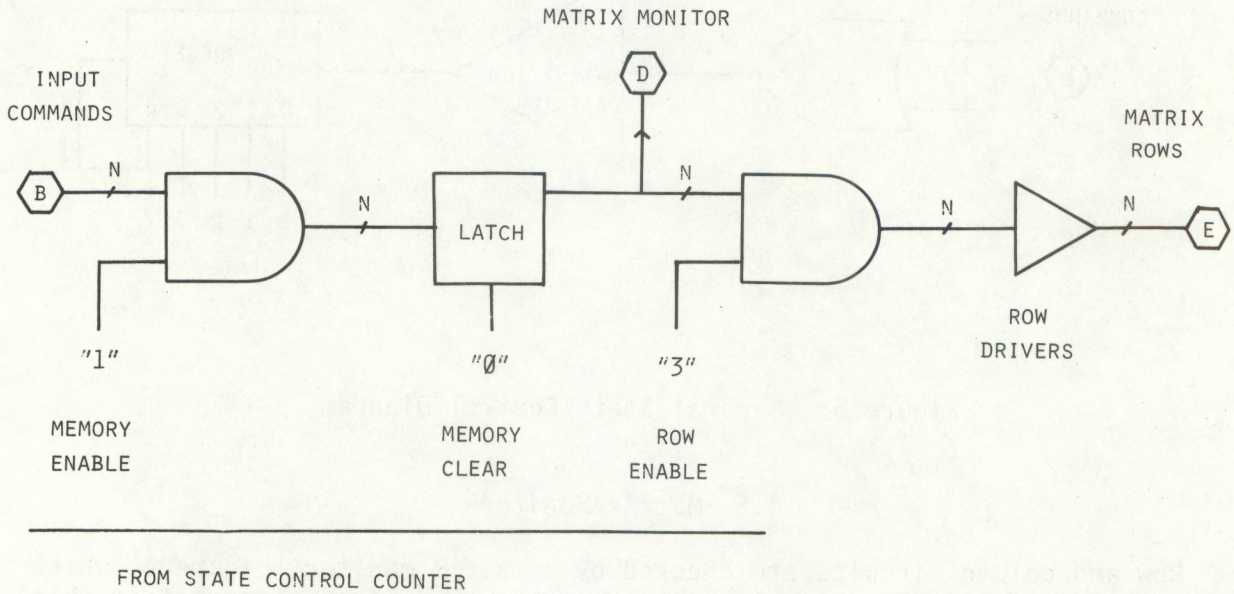


Figure 4. General Form of Row Control Circuit.

"0" is a logic 1 to reset (clear) the memory. When any command is received, one of B's N inputs is a logic one, "0" goes to zero, and "1" becomes one. This allows the appropriate command number to register in memory and be transferred to the matrix monitor. Removing the first command drives "1" to logical zero which prevents distrubing the stored row information with the column selections. Ten seconds after the column has been selected by the second command, "3" goes to logic one enabling the row driver to energize the appropriate relay.

4.4 State Control

The core state control functions are presented in Figure 5. The state control circuit works by counting the transitions beginning and ending any command. Therefore, all N commands are ORed to produce one output which feeds an edge detector. The edge detector's output clocks a base ten counter through four states. The counter resets a "0" before any commands are input by the receiver. It counts the four edges of two commands, and state "4" is used to reset the counter to state "0". Therefore, state "4" exists for less than a microsecond as is functionally identical with state "0". These four states 0 through 3 drive the row control section and time the duration of or between the commands. If a certain sequence is not satisfied, the machine resets to state "0". The times tested are listed in Figure 2.

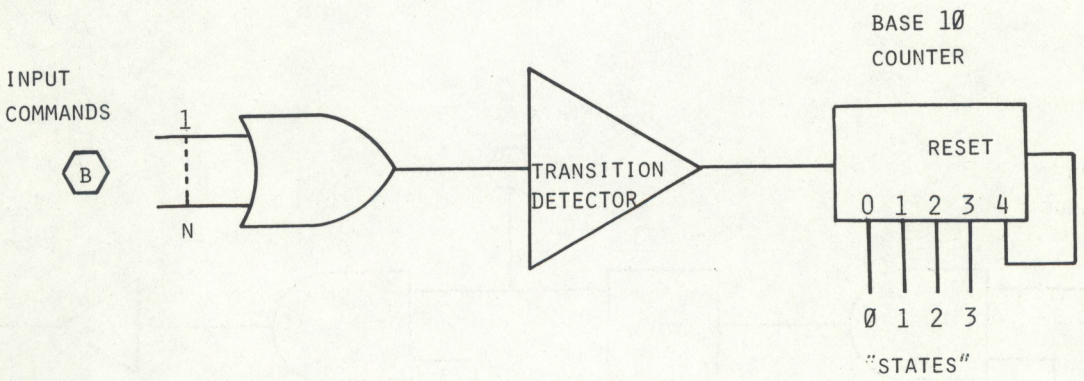


Figure 5. General State Control Diagram.

4.5 Matrix Monitor

Row and column circuits are checked by a matrix monitor, Figure 6, which encodes element selection signals as a three bit word plus an error flag (bit). The flag is set to logic one if multiple commands are present. If the error flag is set, it immediately inhibits the selection of any matrix element. This information is available for transmission to the remote operator so he can observe the circuit's performance.

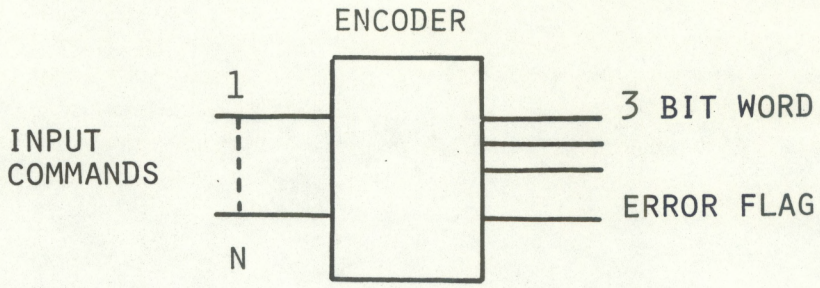


Figure 6. Matrix Monitor for Row or Column.

5. IMPLEMENTATION

The preceding section treated each circuit on a functional level. Here certain details which may not be obvious from the preceding information or from the schematics will be discussed.

Specifically, all prior discussions and figures have used the positive logic convention; for the most part, that follows through to the hardware. However, there are certain cases where De Morgan's theorem was applied to produce the effects described in section 4. For instance, the command receiver relay outputs are form "a" (normally open) contacts with an external pullup resistor. The resulting logic ones are ANDed to produce NOR function which is then inverted to implement the OR gate of Figure 2.

Also, the receiver contacts exhibit bounce and chatter associated with mechanical switches. A debounce circuit includes between the OR gate and the transition detector, precludes extra pulses from entering the state counter.

Most remaining circuits follow the section 4 discussions. As-built schematics, parts lists, etc. are in the appendices.

6. CONCLUSION

This report documents the joining of two proven techniques: the AND matrix and the digital sequential machine to produce a reliable method of substantially increasing the number of independent closures for any given system.

7. ACKNOWLEDGMENTS

Messrs. John Maure and Sam Mares of New Mexico State University's Physical Science Laboratory (BBR) contributed much time and energy, plus many useful suggestions in the development and testing of the device here documented. Mr. Paul Cordery also of BBR suggested the contact debounce DIP.

APPENDIX A

As-built Schematics and Wiring Tables

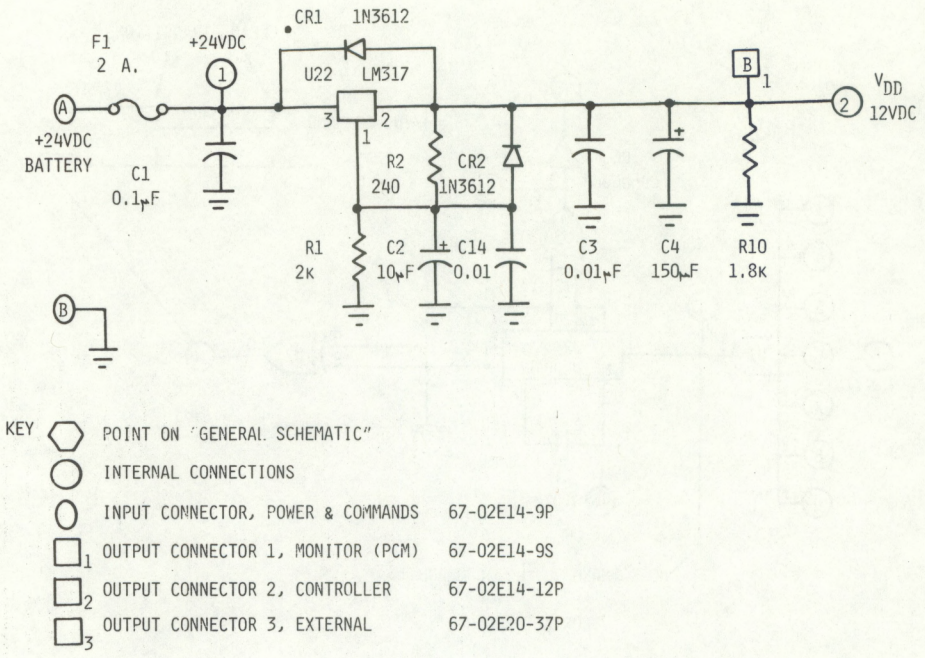


Figure A1. Power Supply and Connector Key (ARL-0002).

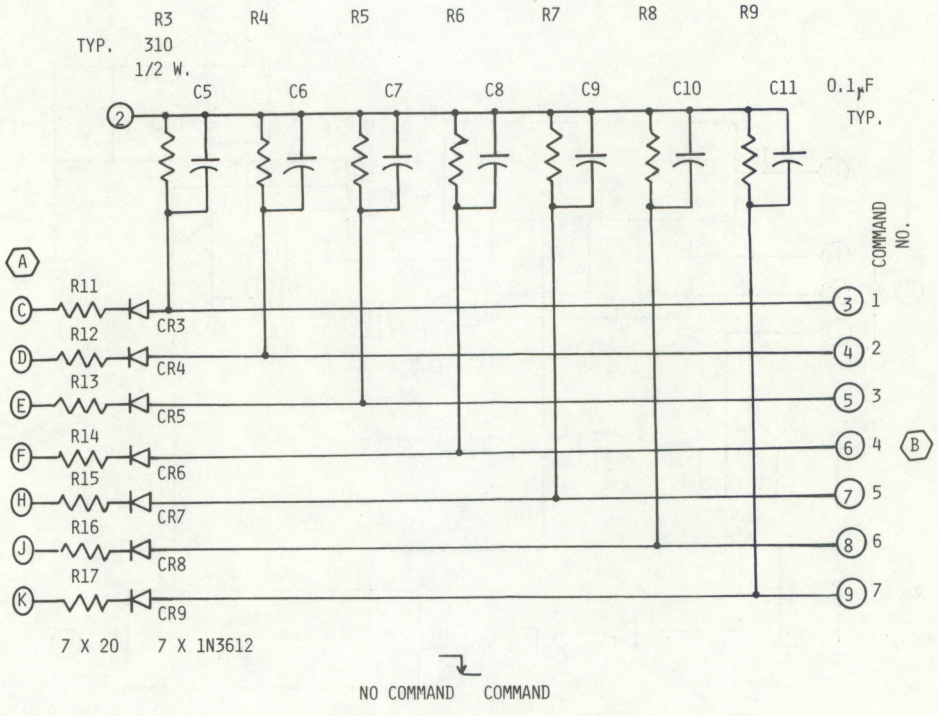


Figure A2. State Control, Command Loads (ARL-0003).

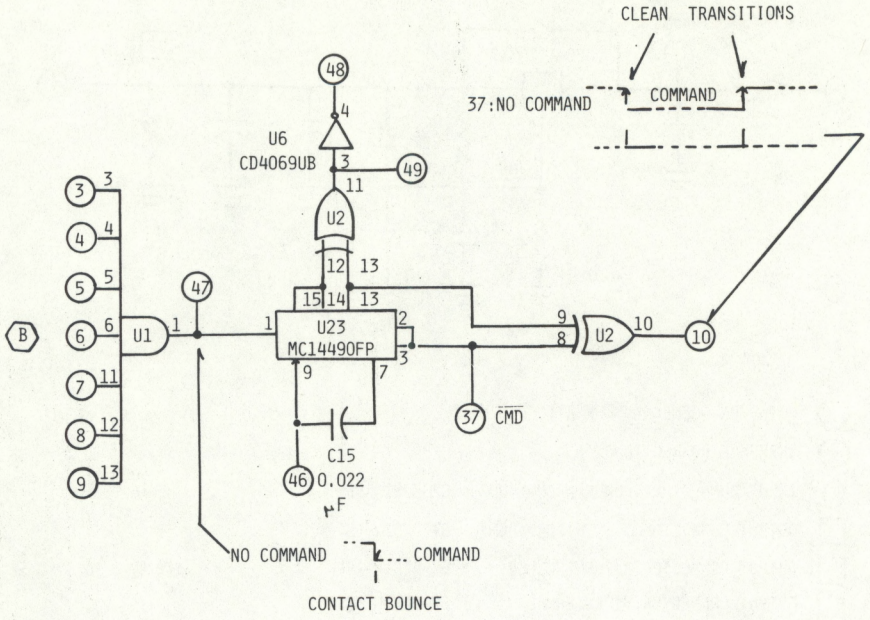


Figure A3. State Control, Detectors (ARL-0004).

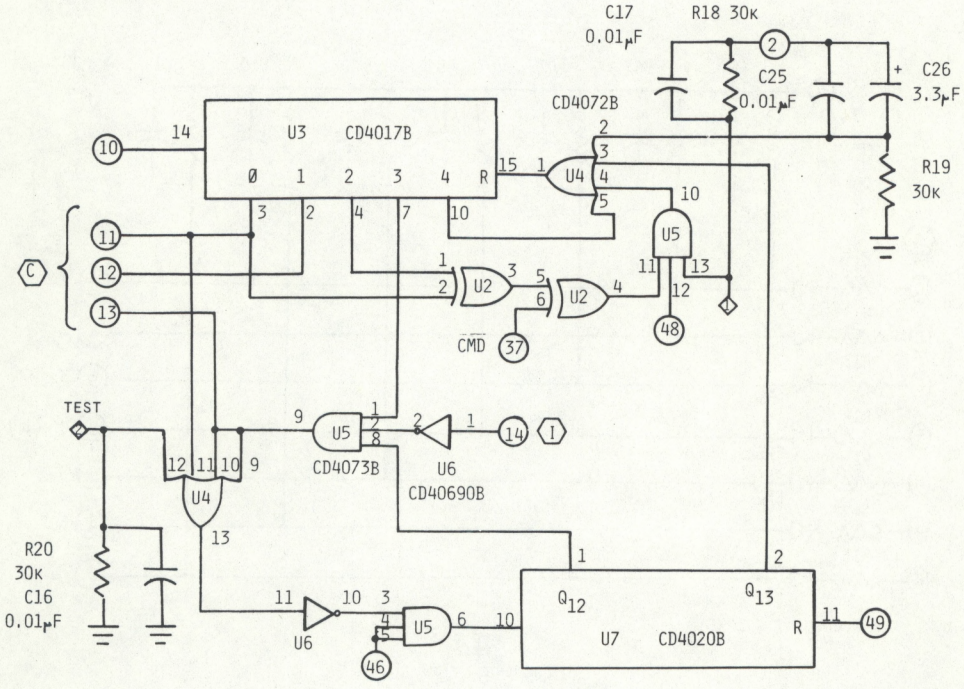


Figure A4. State Control, Counter/Timer (ARL-0005).

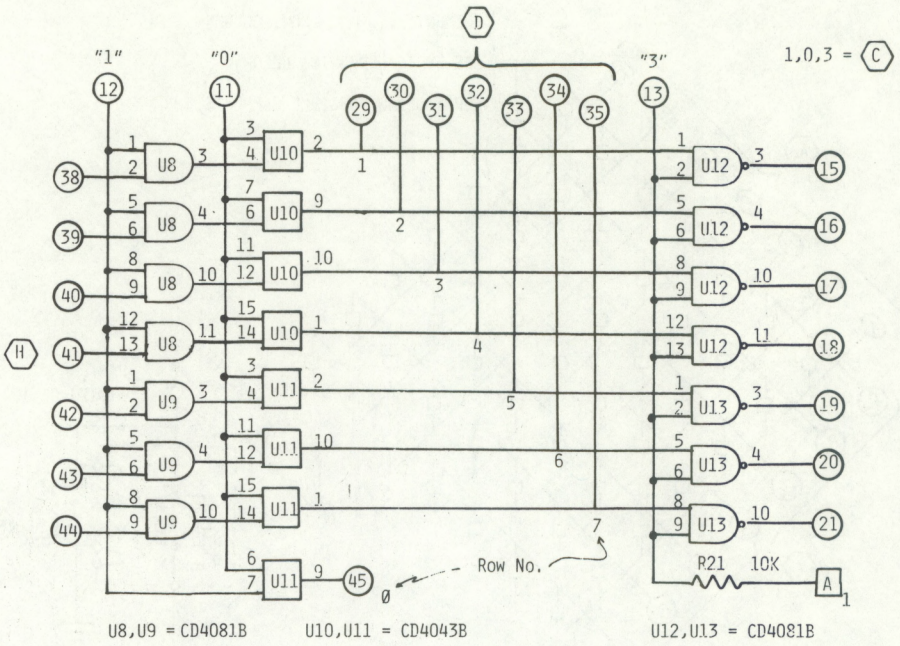


Figure A5. Row Control (ARL-0006).

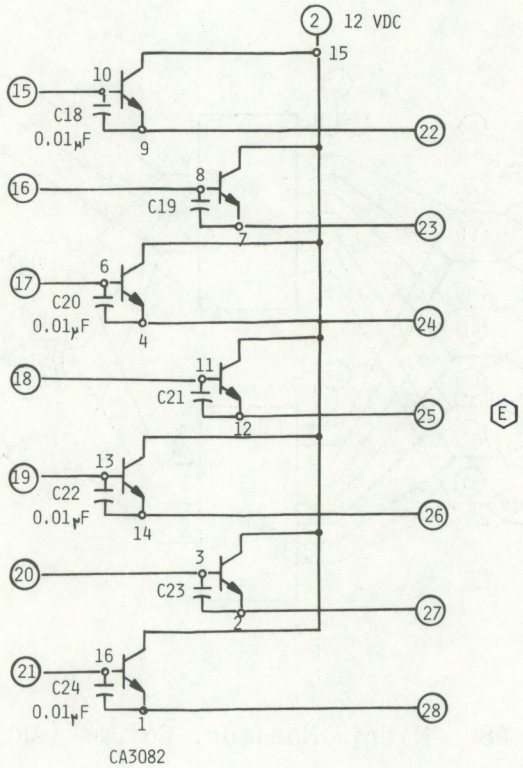


Figure A6. Row Drivers (ARL-0007).

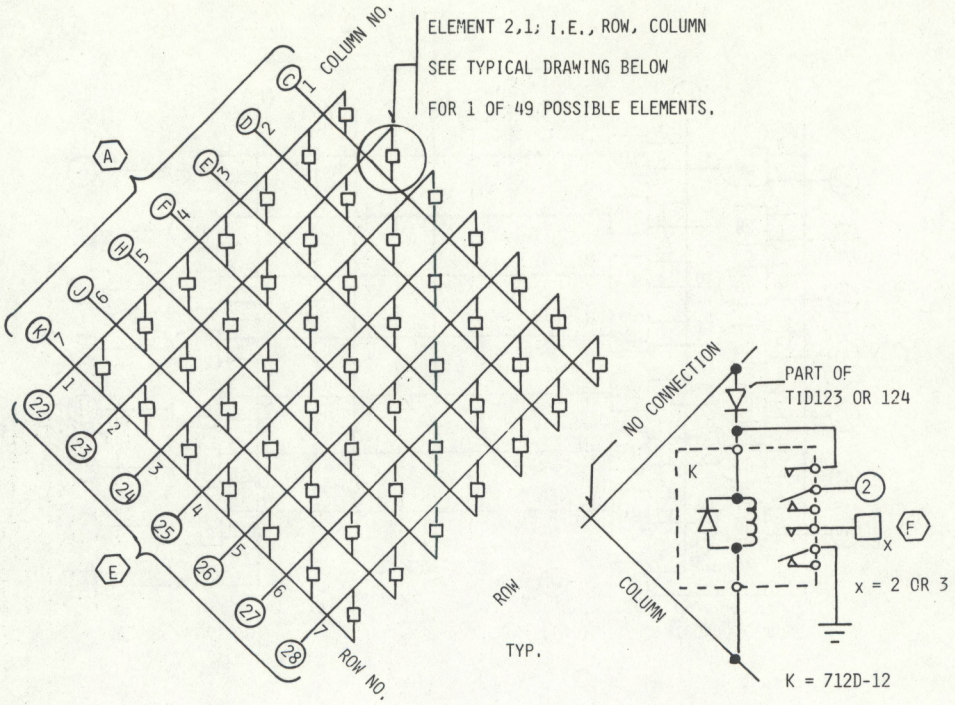


Figure A7. Output Commands (Closures) (ARL-0008).

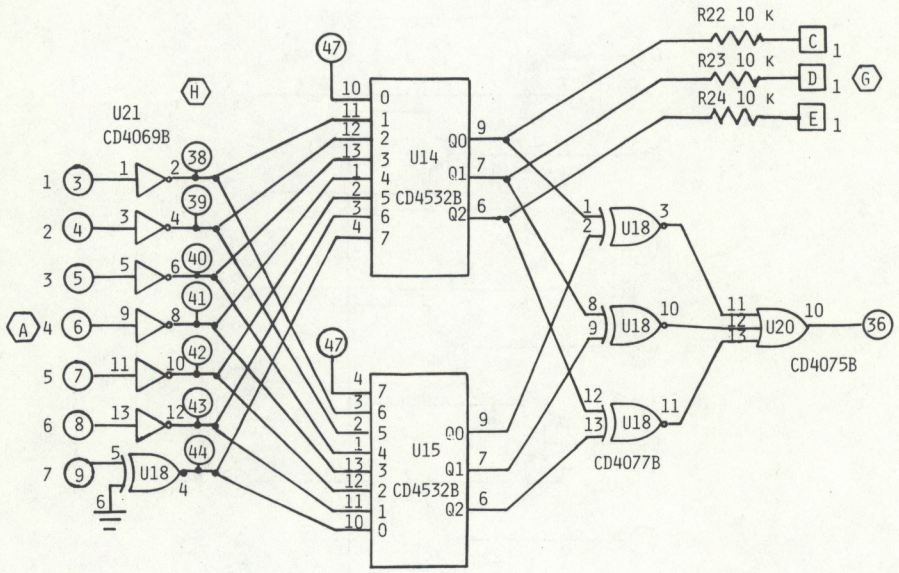


Figure A8. Matrix Monitor, Column (ARL-0009).

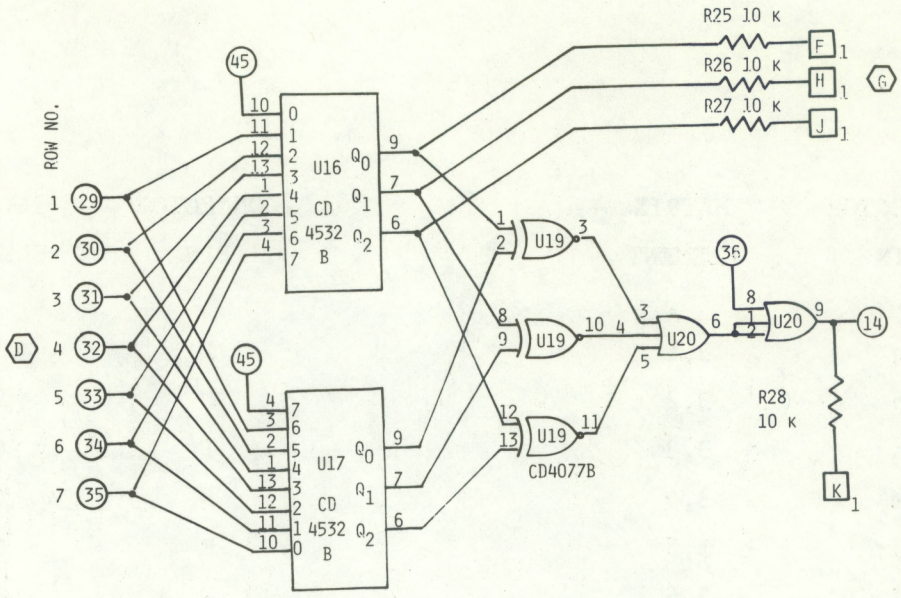


Figure A9. Matrix Monitor, Row and Error Flag (ARL-0010).

CONNECTOR PIN	MATRIX ELEMENT*
N	1,1
M	1,2
L	1,3
K	1,4
J	1,5
H	1,6
F	1,7
E	2,1
D	2,2
C	2,3
B	2,4
A	2,5

*Row, Column

Figure A10. Output Connector 2 (ARL-0014).

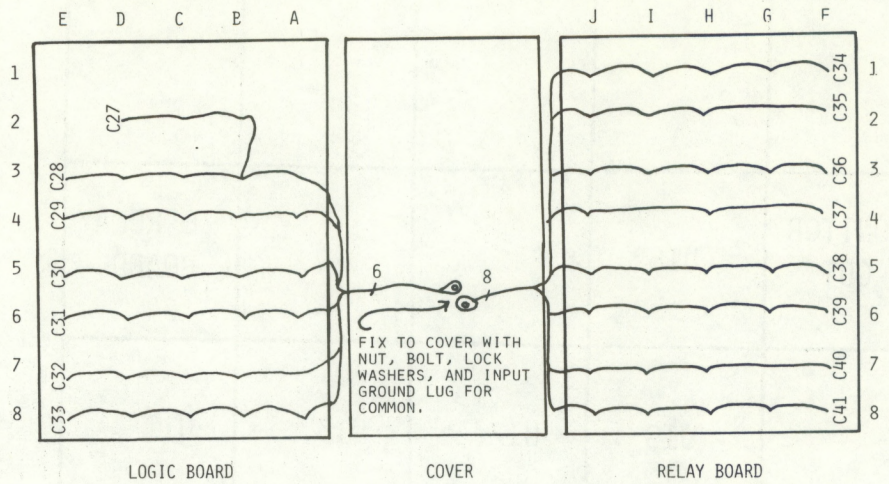
CONNECTOR PIN	MATRIX ELEMENT	CONNECTOR PIN	MATRIX ELEMENT
q	3,1	V	5,6
p	3,2	U	5,7
n	3,3	T	6,1
m	3,4	S	6,2
k	3,5	R	6,3
j	3,6	P	6,4
i	3,7	N	6,5
h	4,1	M	6,6
g	4,2	L	6,7
f	4,3	K	7,1
e	4,4	J	7,2
d	4,5	H	7,3
c	4,6	F	7,4
b	4,7	E	7,5
a	5,1	D	7,6
Z	5,2	C	7,7
Y	5,3	B	2,6
X	5,4	A	2,7
W	5,5		

Figure A11. Output Connector 3 (ARL-0015).

APPENDIX B

Layouts and Wire Routing

1. DRAWING SHOWS GROUND WIRING



2. LOGIC BOARD V_{DD} IS RUN SIMILARLY. A7 AND A5 ARE V_{DD} DISTRIBUTION POINTS.
3. RELAY BOARD V_{DD} IS ALSO SIMILAR WITH G4 PIN 16 FEEDING I1, J3, AND J6 DIRECTLY. I1 FEEDS J2. J3 FEEDS J4 AND J5. J6 FEEDS J7 AND J8. FOR EACH ROW, COLUMN J FEEDS COLUMNS I, H, G, AND F.

Figure B1. Power Wiring (ARL-0053).

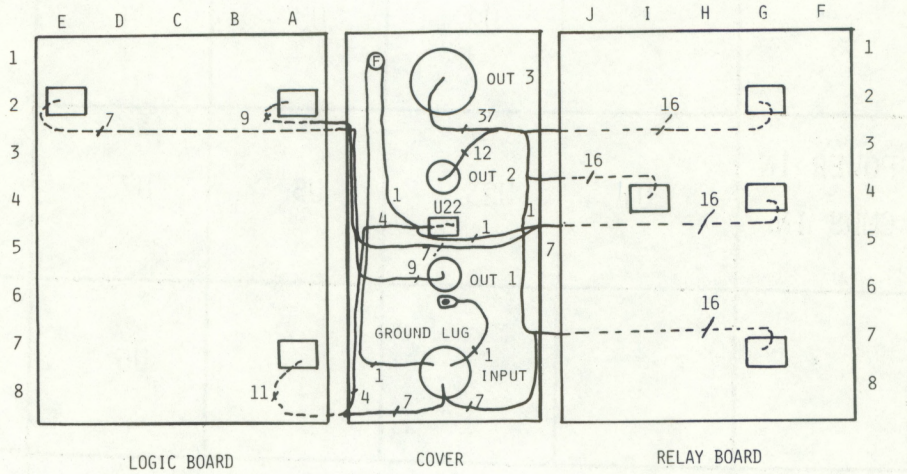


Figure B2. Chassis Harness (ARL-0052).

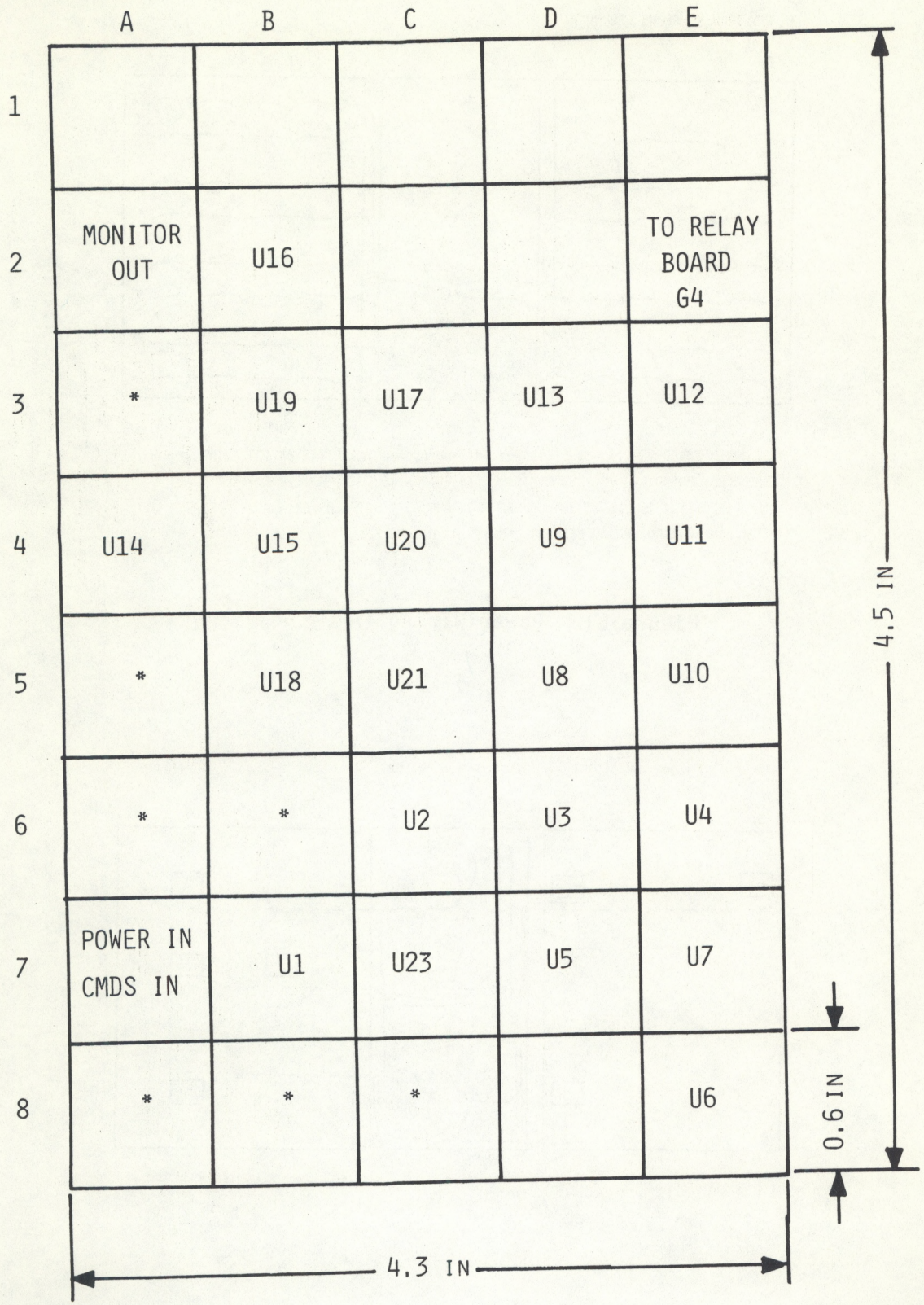


Figure B3. Logic Board Layout (ARL-0042).

BOARD INPUT/OUTPUT CONNECTIONS

PIN NUMBER	CONNECTOR SLOT A7	A2	E2
1	(C)	A	ROW 1
2	(D)	B	ROW 2
3	(E)	C	ROW 3
4	(F)	D	ROW 4
5	(H)	E	ROW 5
6	(J)	F	ROW 6
7	(K)	H	ROW 7
8	U22, 1	J	
9	U22, 3	K	
10	U22, 2		
11	U22, 2		
12	TIE POINTS, V_{DD}		
13			
14			
15			
16			

Figure B4. Logic Board Detail (ARL-0043).

	F	G	H	I	J
1	K1 K2	K3 K4	CR12-CR18	K5 K6	
2	K7 K8	EXIT	CR20-CR26	K9 K10	K11 K12
3	K13 K14	K15 K16	CR28-CR34	K17 K18	K19 K20
4	K21 K22	INPUT & EXIT	U24	EXIT	K23 K24
5	K25 K26	CR36-CR42	*	K27 K28	K29 K30
6	K31 K32	K33 K34	CR44-CR50	K35 K36	K37 K38
7	K39 K40	EXIT	CR52-CR58	K41 K42	K43 K44
8	K45 K46	K47 K48	CR60-CR66	K49 -	

NOTE: SEE ARL-0042 LOGIC BOARD LAYOUT FOR DIMENSIONS.

Figure B5. Relay Board Layout (ARL-0044).

OUTPUT RELAYS VERSUS CONNECTOR AND PIN

		CONNECTOR SLOT			
		G2	G4	I4	G7
PIN NUMBER	1	K1	K17	K18	K34
	2	K2	ROW 1	K19	K35
	3	K3	ROW 2	K20	K36
	4	K4	ROW 3	K21	K37
	5	K5	ROW 4	K22	K38
	6	K6	ROW 5	K23	K39
	7	K7	ROW 6	K24	K40
	8	K8	ROW 7	K25	K41
	9	K9	CMD 1	K26	K42
	10	K10	CMD 2	K27	K43
	11	K11	CMD 3	K28	K44
	12	K12	CMD 4	K29	K45
	13	K13	CMD 5	K30	K46
	14	K14	CMD 6	K31	K47
	15	K15	CMD 7	K32	K48
	16	K16	V_{DD}	K33	K49

Figure B6. Relay Board Detail (ARL-0045).

A3	R21	B6	R7
	R22		C9
	R23		R8
	R24		C10
	R25		R9
	R26		C11
	R27		
	R28		
A5	R10	B8	R3
	C3		C5
	+CR2		R4
	R2 +C4		C6
	+C2		R5
	R1/C14		C7
	CR1+		R6
	C1		C8
A6	R15	C8	C25
	CR7+		+C26
	R16		R19
	CR8+		C15
	R17		R20/C16
	CR7+		R18/C17
A8	R11	H5	C18
	CR3+		C19
	R12		C20
	CR4+		C21
	R13		C22
	CR5+		C23
	R14		C24
	CR6+		

Figure B7. Header Detail. The columns above assume that the headers indicated by the underlined numbers are from the top with the pin 1 in the upper left corner.

APPENDIX C

Parts Lists

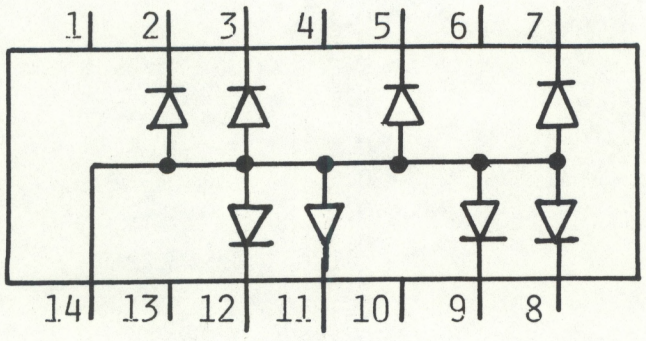
PARTS LIST: CAPACITORS

NUMBER	VALUE (μF)	TYPE*
1	0.1	C
2	10	T
3	0.01	C
4	150	T
5	0.1	C
6	0.1	C
7	0.1	C
8	0.1	C
9	0.1	C
10	0.1	C
11	0.1	C
12	0.01	C
13	3.3	T
14	0.01	C
15	0.022	M
16	0.01	C
17	0.068	M
18	0.01	C
19	0.01	C
20	0.01	C
21	0.01	C
22	0.01	C
23	0.01	C
24	0.01	C
25	0.01	C
26	3.3	T
27	0.1	C
28	0.1	C
29	0.1	C
30	0.1	C
31	0.1	C
32	0.1	C
33	0.1	C
34	0.1	C
35	0.1	C
36	0.1	C
37	0.1	C
38	0.1	C
39	0.1	C
40	0.1	C
41	0.1	C

*C = ceramic T = tantalum M = mica or mylar

PARTS LIST: DIODES

NUMBER	TYPE	DRAWING
1	IN3612	ARL-0002
2	IN3612	-0002
3	IN3612	-0003
4	IN3612	-0003
5	IN3612	-0003
6	IN3612	-0003
7	IN3612	-0003
8	IN3612	-0003
9	IN3612	-0003
10	--	--
11	--	--
12-18	TID123	-0008 ROW 1
19	TID123	-0008 Unused
20-26	TID123	-0008 ROW 2
27	TID123	-0008 Unused
28-34	TID123	-0008 ROW 3
35	TID123	-0008 Unused
36-42	TID123	-0008 ROW 4
43	TID123	-0008 Unused
44-50	TID123	-0008 ROW 5
51	TID123	-0008 Unused
52-58	TID123	-0008 ROW 6
59	TID123	-0008 Unused
60-66	TID123	-0008 ROW 7
67	TID123	-0008 Unused



TID 123, TID 124

14 PIN DIP

PARTS LIST: INTEGRATED CIRCUITS

NUMBER	TYPE		CONNECTIONS	
	PRIMARY	SECOND	V_{SS}	V_{DD}
1	CD4048A		8,15,7,9	16,2,10,14
2	CD4070B		7,	14
3	CD4017B		8,13	16
4	CD4072B		7	14
5	CD4073B		7	14
6	CD4069UB	CD4049	7	14,13,9,5
7	CD4020B	CD4040B	8	16
8	CD4081B		7	14
9	CD4081B		7	14,13,12
10	CD4043B		8	16,5
11	CD4043B		8	16,5
12	CD4081B		7	14
13	CD4081B		7	14,13,12
14	CD4532B		8	16,5
15	CD4532B		8	16,5
16	CD4532B		8	16,5
17	CD4532B		8	16,5
18	CD4077B		7,6	14
19	CD4077B		7,6,5	14
20	CD4075B		7	14
21	CD4069B	CD4049B	7	14
22	LM317		--	2
23	MC14490FP		8,10,5,12	16
24	CA3082	ULN2082	5	15

PARTS LIST: RELAYS

RELAY NUMBER VERSUS MATRIX ELEMENT*

ROW NO.	COLUMN NO. 1	2	3	4	5	6	7
1	1	2	3	4	5	6	7
2	8	9	10	11	12	13	14
3	15	16	17	18	19	20	21
4	22	23	24	25	26	27	28
5	29	30	31	32	33	34	35
6	36	37	38	39	40	41	42
7	43	44	45	46	47	48	49

*Matrix Element - Row, Column

All relays are Teldyne 712D-12 or Hi-G CAWD-12

PARTS LIST: RESISTORS

NUMBER	VALUE (Ω)	WATTAGE*
1	2k	
2	240	
3	310	1/2
4	310	1/2
5	310	1/2
6	310	1/2
7	310	1/2
8	310	1/2
9	310	1/2
10	1.8k	
11	20	
12	20	
13	20	
14	20	
15	20	
16	20	
17	20	
18	30k	
19	30k	
20	30k	
21	10k	
22	10k	
23	10k	
24	10k	
25	10k	
26	10k	
27	10k	
28	10k	

*1/4 W. unless noted

APPENDIX D

Diagnostic Waveforms

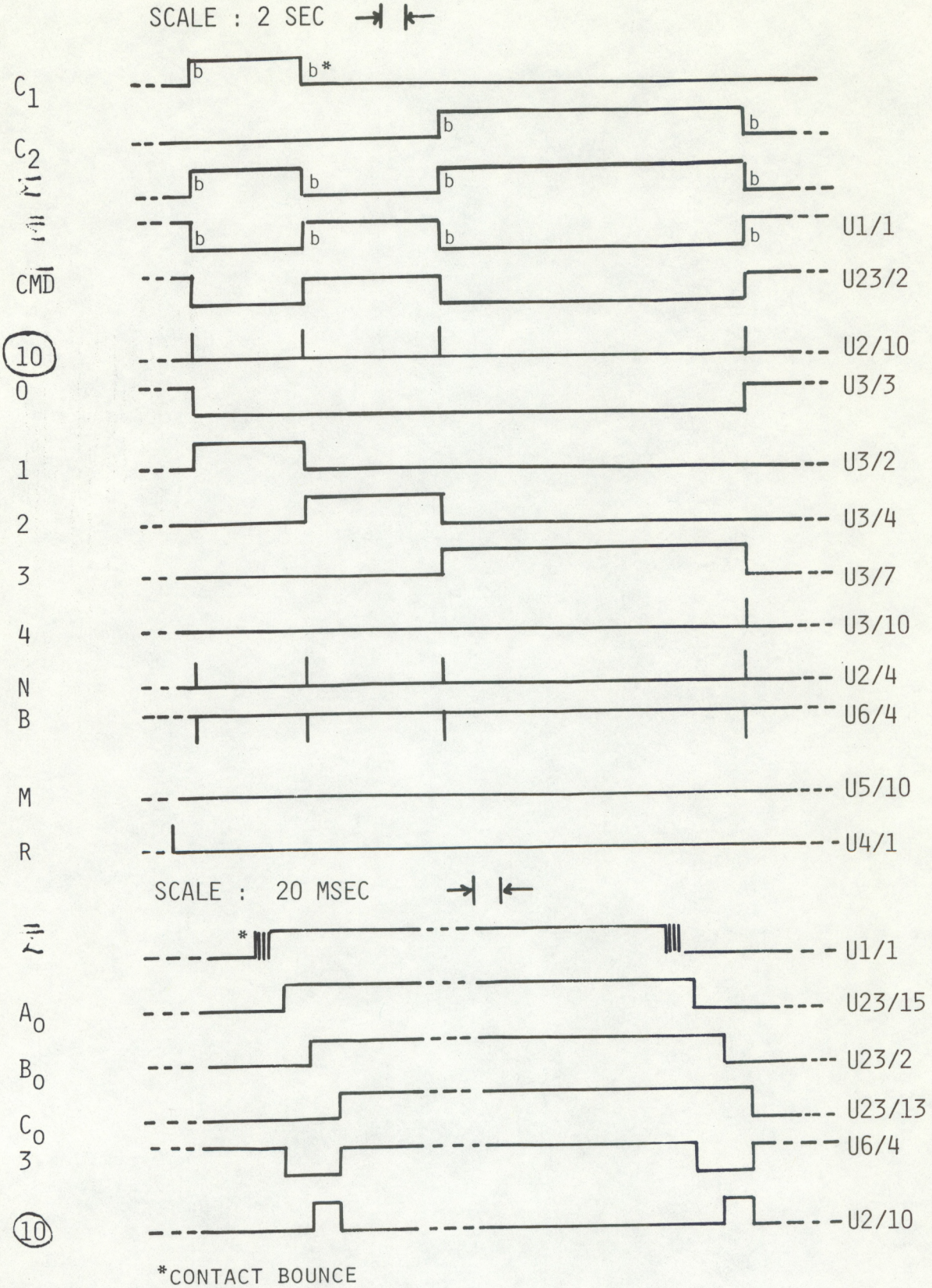


Figure D1. Diagnostic Waveforms (ARL-0041).

APPENDIX E

Photograph