Woods Hole
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A DIGITAL RECORDING SYSTEM FOR MARINE EXPERIMENTATION

By

J. Kim Vandiver

September 1973

TECHNICAL REPORT

Prepared for the National Oceanic Atmospheric Administration - Sea Grant #2-35252.

WOODS HOLE, MASSACHUSETTS 02543

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Approved for Distribution Earl E. Hays
Earl E. Hays, Chairman
Department of Ocean Engineering

"A Digital Recording System For Marine Experimentation"

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J. Kim Vandiver

ABSTRACT

A digital recording system is presented as an alternative to the cumbersome and expensive strip chart recording and magnetic tape techniques presently in use to collect data from "in situ" marine experiments. The complete logic and circuit design of a 64 word by 8 bit memory is presented. The design utilizes CMOS integrated circuits exclusively, fits on a single 4" X 6" printed circuit card, and can be potted for protection. Wide temperature range and low power consumption make it suitable for applications in any marine environment.

ACKNOWLEDGEMENTS

This work was sponsored in part by the continuing program of graduate education in the Ocean Engineering Department at Woods Hole Oceanographic. Additional support was provided from N.S.F. Grant GA 31987, "Instrumentation for Biological Oceanography." As the principle investigator for this grant, Dr. John Kanwisher recognized the need for improved data collecting techniques for "in situ" marine biological experiments, and first suggested that I design a small digital recording system. He further supported my work by providing laboratory space, materials, test equipment and frequent encouragement.

Particular credit must be given to Neil Brown, who was most generous in sharing with me his design ideas for a digital data collecting system. His ideas formed a nucleus from which the present design evolved.

As with any design project, the day to day crises at the work bench had to be resolved. At these times I turned to Ken Lawson. His electrical engineering expertise solved some of my most perplexing problems. More important, he is a most capable and enthusiastic teacher.

My thanks also go to numerous people in the W.H.O.I. community who helped prepare and publish this report.

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LIST OF KEY WORDS AND SYMBOLS

Write	To place a word into the memory
Read	To extract a word from the memory
Strobe	A timing signal to the memory to allow reading or writing
CMOS	Complimentary Metal Oxide Semiconductor
usec	Microsecond
msec	Millisecond
$\emptyset_1$	Phase one of clock
$\emptyset_2$	Phase two of clock
0	Low logic state, electrical ground $-V_{SS}$
1	High logic state, electrical positive $-V_{DD}$
$D_8 \ldots D_1$	Binary number composed of 8 bits
MSB	Most Significant Bit of a binary number
LSB	Least Significant Bit of a binary number
NAND	A logic Not And
NOR	A logic Not Or
Inverter	A logic Compliment

I. INTRODUCTION

Small scale marine experiments are often seriously restricted by current methods of data storage. A bell jar placed on the sea bottom to measure and record oxygen productivity is an example. The choice of recording equipment has been generally limited to magnetic tape or strip chart recorder. Both require bulky, watertight packaging that must be opened periodically for servicing and data retrieval. Flooded instruments are an inevitable result.

One alternative is to continuously transmit the data by acoustic telemetry. This still requires a person, or recording mechanism on site 24 hours per day. Recent availability of random access digital memories on large scale integrated circuit chips has provided a low cost, easily packaged alternative. These allow data to be accumulated in a form that is readily available for nondestructive readout. Transmission over the telemetry link can then be scheduled at the convenience of the experimenter.

The circuit that is described in the following report is a digital data recording package, complete with all necessary input, output and control lines. It is capable of storing 64, 8 bit binary numbers, such as oxygen measurements. If one measurement were stored every 22.5 minutes, then 24 hours of data could be stored in the memory.

Data retrieval can be accomplished by retrieving the instrument, by daily acoustic transmissions that are regulated by a digital clock in the instrument package, or by acoustic transmission on command from a coded acoustic source operated on the surface.

Data output consists of 64, 8 bit numbers, beginning with the most significant bit (MSB) of the oldest number and ending with the least significant bit (LSB) of the most recent number. Acoustically the individual bits might be high and low tones, corresponding to 1 and 0 logic states. Provision is made for separating each 8 bit number with any 2 bit combination of spaces, 1's or 0's.

Readout does not destroy the data in the memory, and the data may be read out more than once. After the 64th word has been transmitted, the memory returns to the task of additional data acquisition. When the 65th data point is read into the memory, it takes the place of the oldest word. This replacement of the oldest word with the most recent word continues as long as data is presented to the memory. The memory is organized like a wheel with 64 word positions on the perimeter. At any time only the last 64 data points presented to the memory will be preserved.

The advantages of this system are numerous:

1. Small, a single 4" X 6" printed circuit card.
2. Inexpensive, less than Rustrak or cassette recorders.
3. No moving parts, total electrical nature of the unit allows it to be potted for waterproofing.
4. Low power requirement, less than one milliwatt.
5. Wide power supply voltage range, 5-15 VDC.
6. Insensitive to temperature fluctuations, -40°C to 125°C.

II. GENERAL FEATURES OF A COMPLETE MEASUREMENT & RECORDING SYSTEM

Figure 1 is a block diagram of a complete instrument. It is intended, for example, to measure, record and transmit the values of

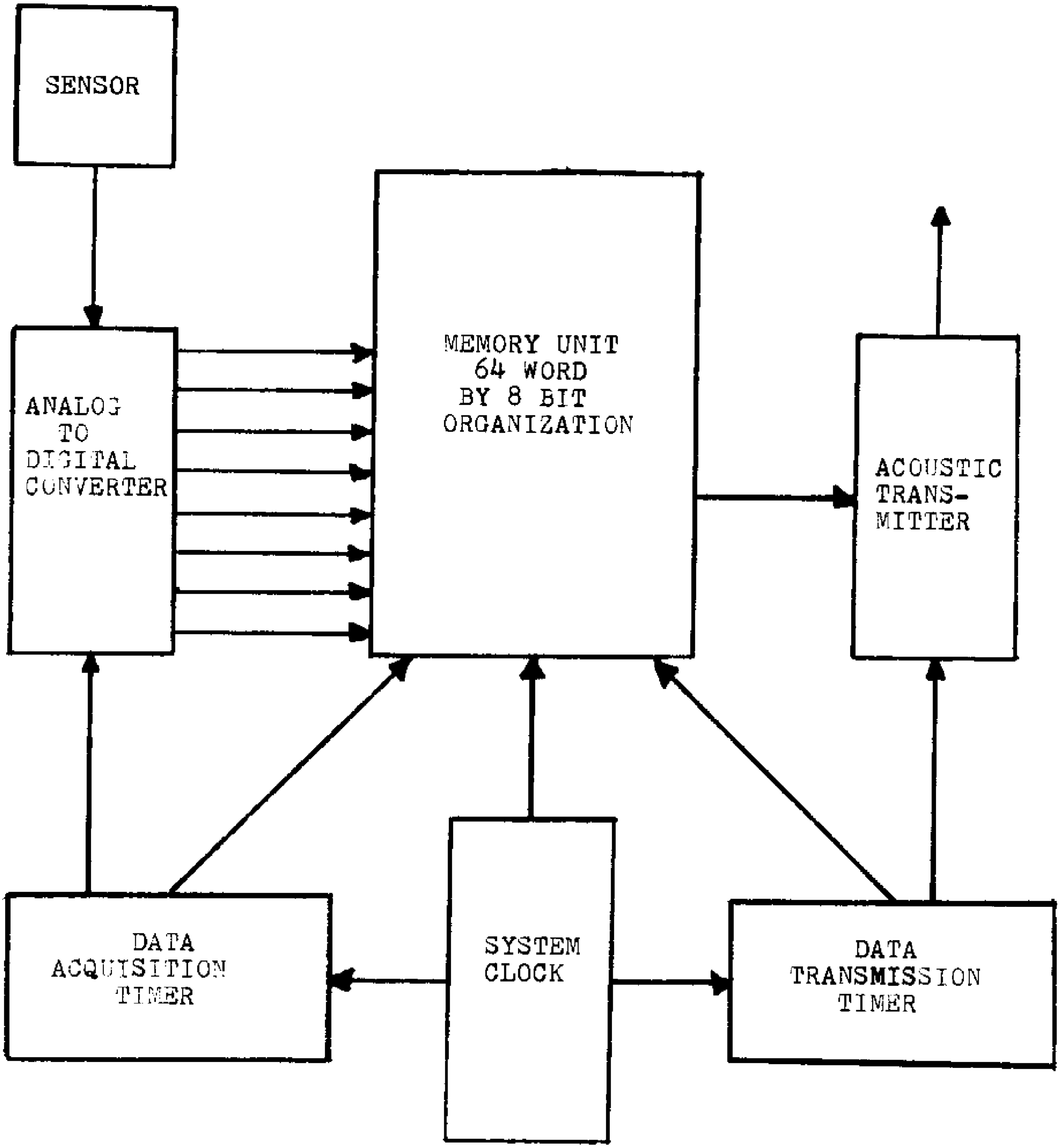

Figure 1. System Block Diagram

dissolved oxygen partial pressure. The instrument has a built-in timer, which turns on an acoustic transmitter every 24 hours.

The heart of the package is a clock, which may be a crystal oscillator for high precision or a simple astable multivibrator. The clock frequency is typically 1 KHz. The clock provides the timing for the memory unit.

The data acquisition timer is a simple binary ripple counter, counting at the clock frequency. The appropriate counter outputs may be chosen to generate a pulse every 22.5 minutes. This pulse causes the memory unit to accept a data point. The data is available on 8 parallel output lines of an A/D converter. The analog input to the converter comes from the oxygen sensor. The entire data acquisition cycle takes 2 clock periods. If the clock is 1 KHz, then the number will be stored in 2 milliseconds.

The data transmission timer can be part of the same binary counter as the acquisition timer. The output is chosen to provide a pulse every 24 hours. This pulse to the memory unit will cause it to send the 64 numbers it contains to the acoustic transmitter. It does this in serial fashion, beginning with the MSB of the oldest number. The bits come out of the memory at the basic clock frequency divided by 1024. If the clock is a 1 KHz clock, then the bits come out at approximately 1 per second.

Each word consists of 8 bits, preceded by two selected spacing bits. The transmitter sends out these bits as high and low tones. The spacing bits can be inhibited at the transmitter to create silent spaces between words. On the surface the data may be transcribed manually or recorded on tape, or both. The details of possible transmitter memory inter-connections are covered in the application notes. After transmitting

64 words the memory returns to the acquisition mode to wait a new data point.

Data transmission may take up to the data acquisition interval, without losing an incoming data point. The memory cannot transmit and acquire data simultaneously, but it will hold an incoming acquisition or transmission request until it is free to process it.

The memory unit, as shown on the block diagram, will be described in detail in the next section. The inputs to it, as shown on the block diagram, are assumed to be available. The other components on the block diagram must be tailored to fit each application and will not be covered in detail.

III. MEMORY UNIT DESIGN SPECIFICATIONS

The memory unit consists of 12 CMOS integrated circuits mounted on a 4" X 6" printed circuit board. There are no other circuit elements, such as capacitors or resistors; and consequently, the total power requirement is extremely low. The input/output connections are made via 21 stake pins mounted on the board.

Figures 2 and 3 are the logic diagram and the timing diagram for the memory unit. The function of the unit will be described by following through a complete data acquisition or "write" cycle and a complete transmission or "read" cycle on these two diagrams. In addition the input and output specifications of the memory unit will be given. The I/O lines will be assigned identification numbers. These numbers appear on Figure 4, the printed circuit layout. Table 1 lists the name and number of the I/O lines. The events on the timing diagram are numbered and will be referred to in the text.

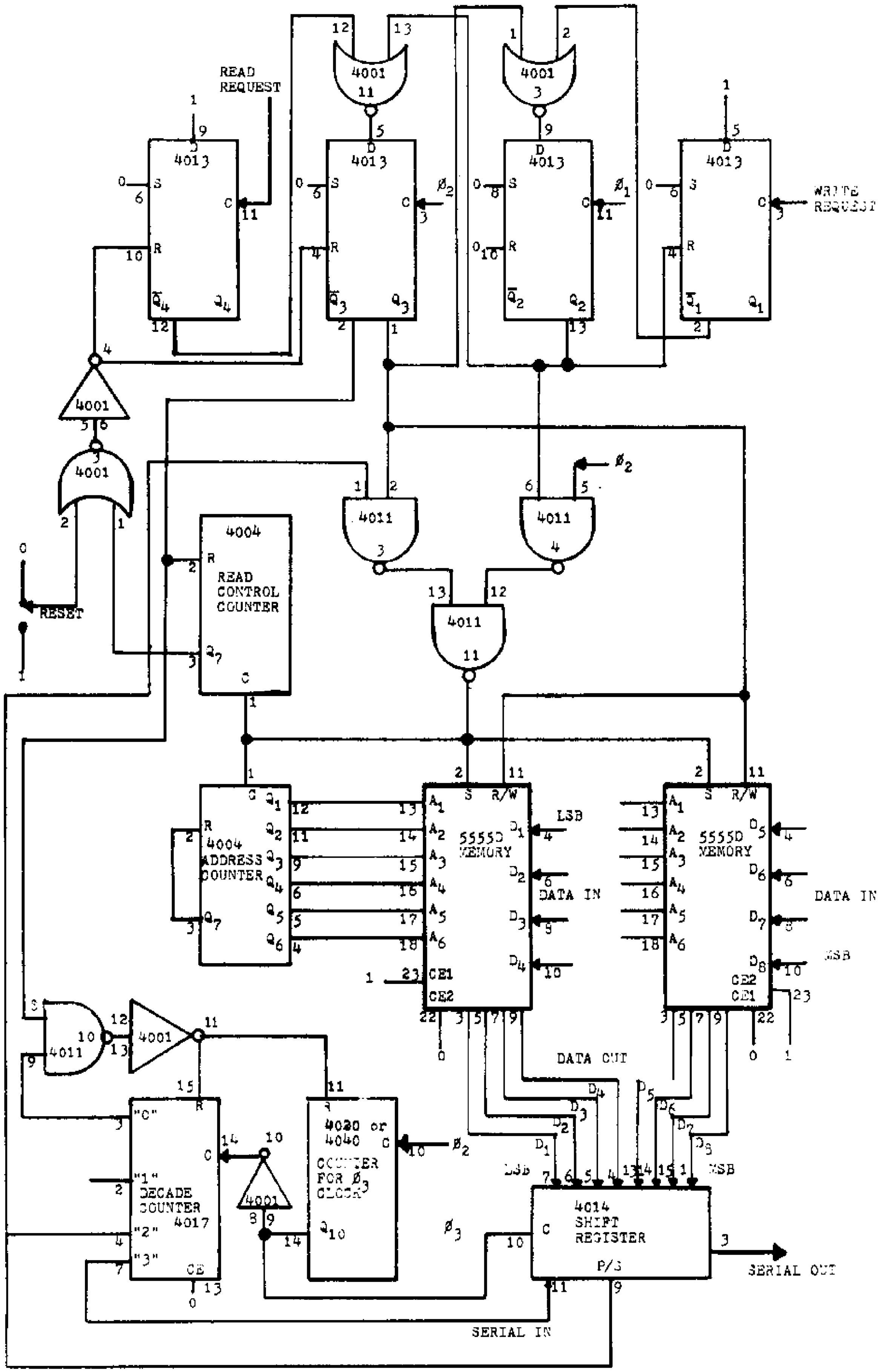

Figure 2. Logic Diagram

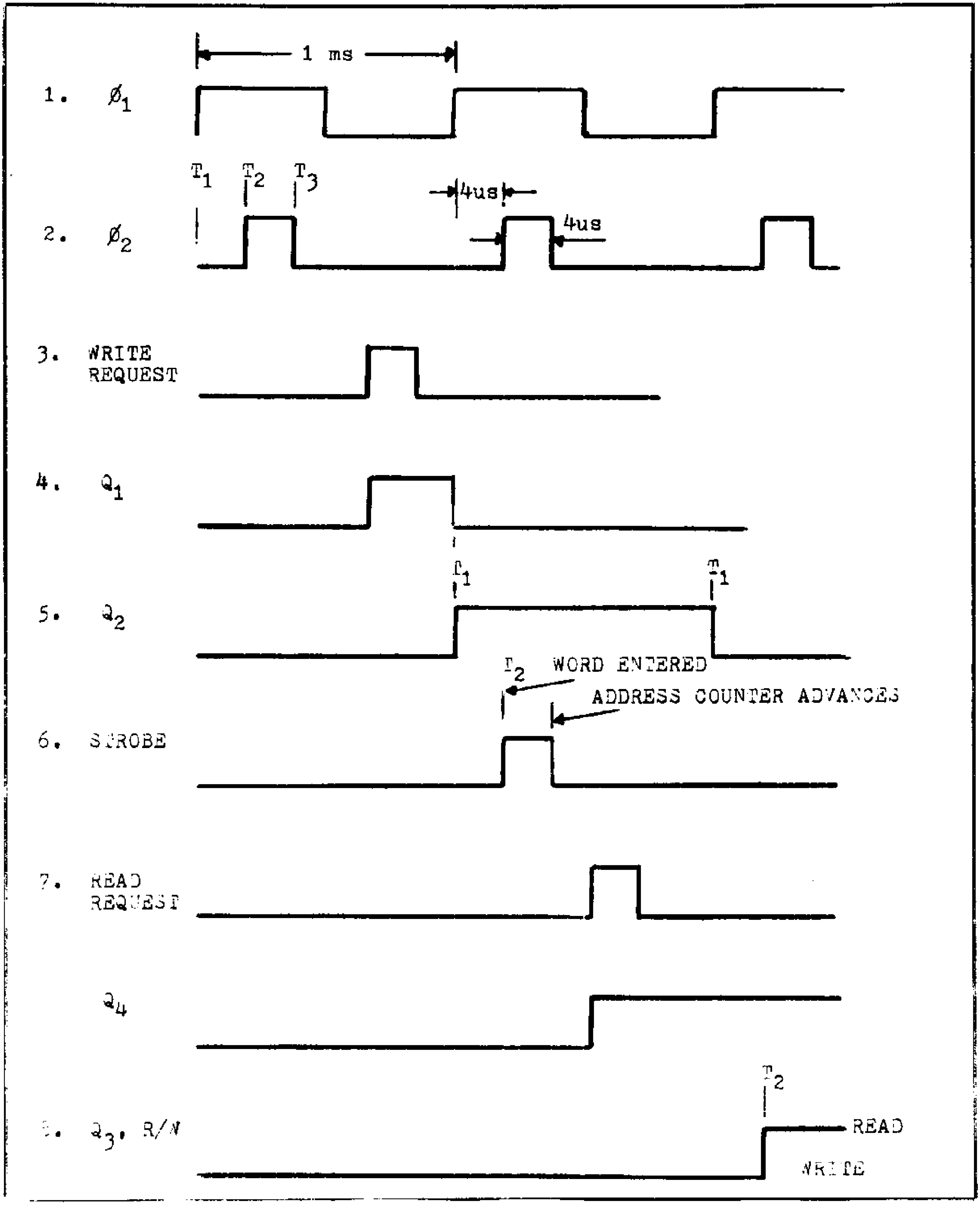

Figure 3A. Timing Diagram

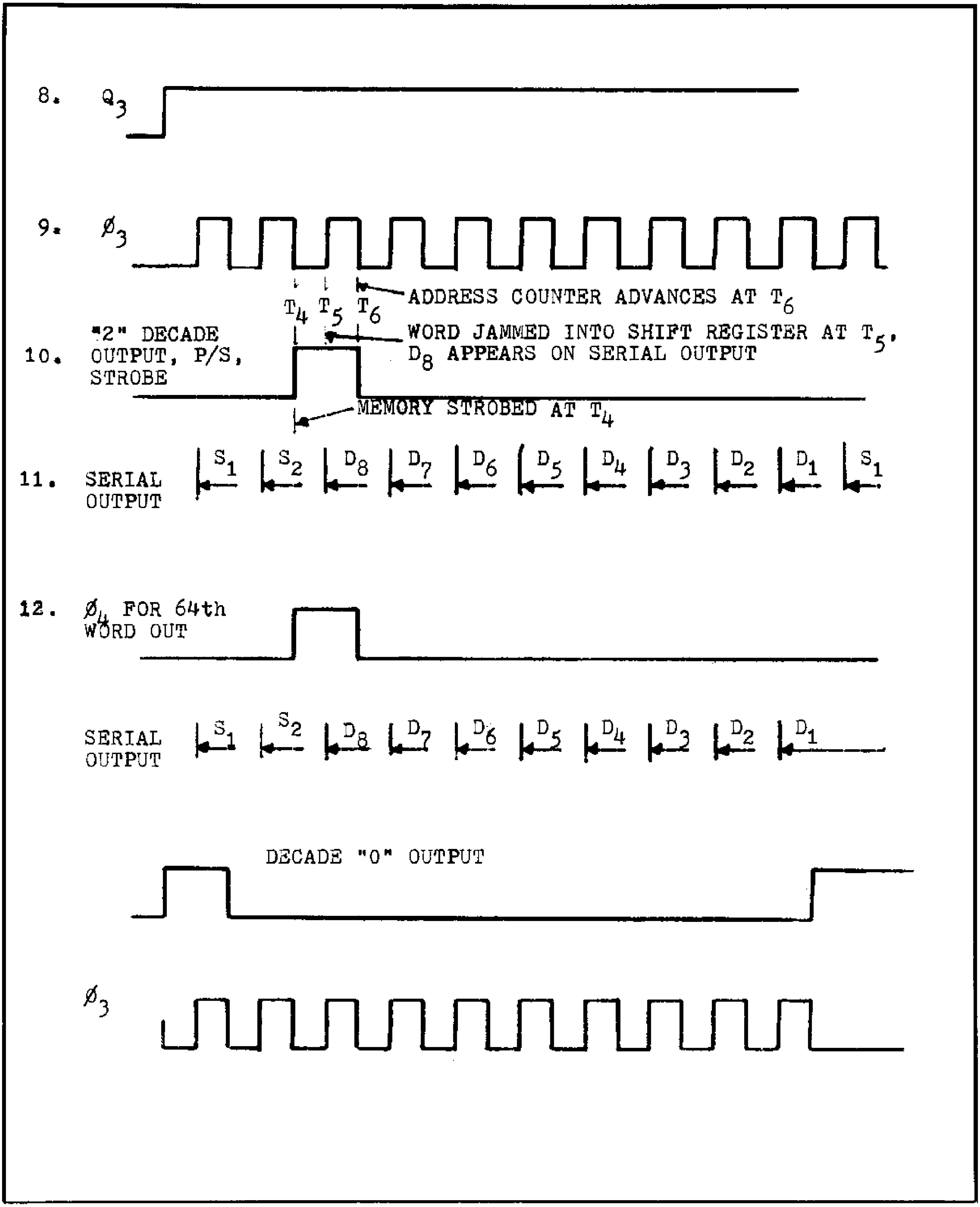

Figure 3B. Timing Diagram

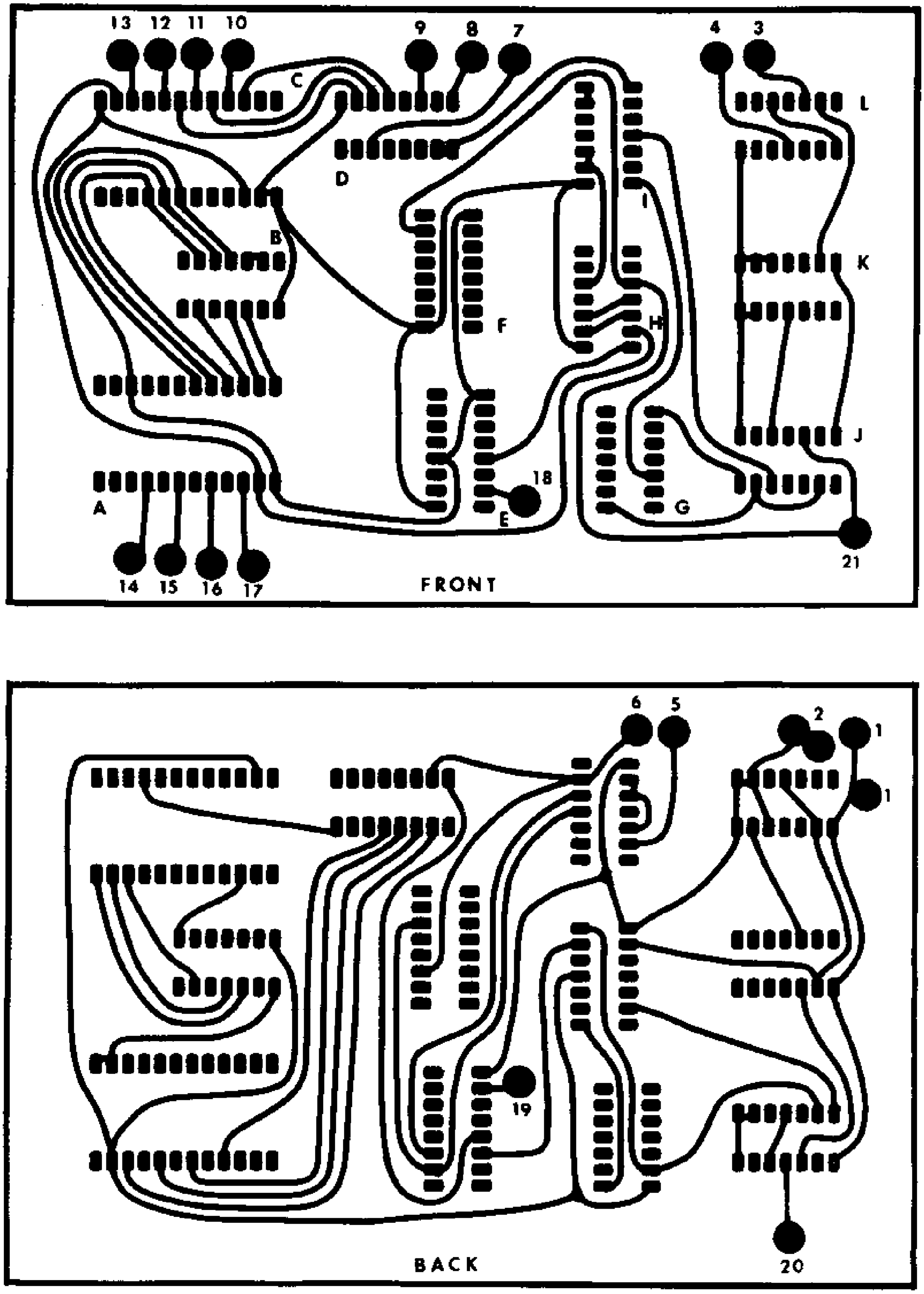

Figure 4. Printed Circuit

TABLE 1

INPUT/OUTPUT LINES TO THE MEMORY UNIT

1. V_{DD} - Positive power input, 5 to 15 VDC.
2. V_{SS} - Negative power supply, 0 VDC.
3. Data acquisition command input.
4. ϕ_1 - Clock input, phase 1.
5. Reset input line.
6. ϕ_3 - Clock output at bit frequency, $\phi_1/1024$.
7. Serial data output line.
8. "2" output from decade counter parallel/serial control to shift register.
9. Serial input to shift register for coding of 2 spacing bits between output numbers.
10. D_5 }
11. D_6 }
12. D_7 }
13. D_8 (MSB) }
14. D_1 (LSB) }
15. D_2 }
16. D_3 }
17. D_4 }

Data input lines.
One input binary number consists of D_8, D_7, $D_6 \ldots D_1$.

18. "1" output from decade counter.
19. "3" output from decade counter.
20. Data transmission request input.
21. ϕ_2 - Clock inputs, phase 2.

Read/Write Request and Control

The left hand side of the logic diagram shows four D-type flip-flops. Their outputs are Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$, etc. The bars above the characters refer to inverted outputs.

Flip-flops 1 and 2 control data acquisition, and 3 and 4 control data transmission.

A single positive "write" pulse to C_1, the clock of flip-flop 1, causes Q_1 to go high.

If the memory is not engaged in a read cycle, Q_2 will go high and cause the memory to accept a data point.

Similarly, an incoming "read" pulse to C_4, the clock of flip-flop 4, will cause Q_4 to go high. If a write cycle is not in progress, Q_3 immediately follows, and the memory begins to read out 64 numbers. Q_2 and Q_3 are interconnected through NOR gates so as to prevent both from being high simultaneously. This prevents the memory from being interrupted during a read cycle by a write request and vice-versa. If a write request comes in during a read cycle, Q_1 will go high and remain there until the read cycle is finished; and the write cycle, though delayed, can commence. Similarly, a read request will wait until a write cycle finishes.

Clock Inputs

1, 2. The basic clock input requirements are referred to as ϕ_1 and ϕ_2. ϕ_2 has the same frequency as ϕ_1, but the positive transistion is delayed. In the test model ϕ_1 was $\sim$1 KHz and was generated by an astable multivibrator. ϕ_2 was delayed 4 μs and was 4 μs wide. The width of ϕ_2 is not important but must be long enough to provide sufficient switching time for CMOS circuitry. T_1 and T_2 refer to positive transitions of ϕ_1 and ϕ_2. T_3 is the negative transition of ϕ_2.

Write Cycle

3. When the external digitization is completed and an 8 bit word is ready for storage, a write request pulse must be sent to the write request input line. The timing is not important.

4. The positive transition of the write request pulse causes Q_1 to go high.

5. At T_1, the time of positive transition of the ϕ_1 clock, Q_2 will go high. A high on Q_2 causes three events to occur.

   a. Q_1 is reset.

   b. Q_3 is prevented from going high.

   c. Q_2 goes to one input of a two input NAND gate. The other input is ϕ_2.

At T_2 an inverted ϕ_2 pulse exits this gate and is inverted by a second NAND gate, whose other input is high.

6. This positive ϕ_2 pulse strobes the word that has been provided on the 8 input data lines into the memory at T_2. At T_3 the address counter advances 1 count. At the following T_1, Q_2 goes low, and the write cycle is complete. The write cycle takes two ϕ_1 clock periods to complete. Hence, $F_{\text{write max}} = \phi_1/2$. The state of Q_3 controls the R/W mode of the memory. The memory is always in the write mode, except when Q_3 is high and readout is in progress.

Read Cycle

7. A read request is made during the write cycle, Q_4 goes high.

8. Q_3 is prevented from going high and thus starting the read cycle, until Q_2 goes low at T_1. Q_3 goes high at T_2 because the clock to the Q_3 flip-flop is ϕ_2. When Q_3 goes high, the reset lines to the read control counter, the divide by 2^{10} ripple counter, and the decade counter

all go low. The read/write control on the memories goes to Read.

9. The divide by 2^{10} counter has $\emptyset_2$ as a clock input. The counter is initially at all zeros. After 2^9 clock pulses the Q_{10} output goes high. For $\emptyset_2$ = 1 KHz, this takes about 1/2 second. Thereafter, the Q_{10} output goes high once each second, or every 2^{10} $\emptyset_2$ input pulses. This one second period clock is identified as $\emptyset_3$.

10. $\emptyset_4$ is the "2" output from a decoded decade counter, that is, initially at "0". $\overline{\emptyset}_3$, the inverted $\emptyset_3$ clock, is the input to the decade clock. The decade counter counts on positive clock transitions. The "2" output goes high 2 seconds after the reset line goes low. $\emptyset_4$ stays high for 1 input clock period. In this case, 1 second. It then goes low for 9 periods. The same is true for other decade counter outputs. When the "2" goes low, then the "3" goes high for 1 period, etc. $\emptyset_4$ is the P/S, parallel/serial, control for the shift register. When $\emptyset_4$ is high, the shift register will jam in whatever is on the parallel input lines at the positive transition of the clock input. The clock input is $\emptyset_3$. $\emptyset_3$ goes high in the middle of the 1 second long $\emptyset_4$ pulse.

The $\emptyset_4$ pulse is also gated through a two input NAND gate. The other input is Q_3 and is high. The output is inverted by a second NAND gate. The $\emptyset_4$ pulse strobes the memory at T_4. The word that is currently addressed by the address counter is made available on the parallel out lines for the duration of the high $\emptyset_4$ pulse, which is one second in this example. In the middle of this period, at T_5, the shift register accepts the number. On the negative transition of $\emptyset_4$, T_6, the address counter, is advanced one count. The read control counter also advances one count at T_6.

Serial Out Data

11. The "2" output from the decade counter is $\emptyset_4$. It serves as the parallel/serial control on the shift register as well as the strobe for

the memory. When $\emptyset_4$ goes high, the memory presents the currently addressed word on 8 parallel data out lines. These 8 data lines go to parallel inputs on an 8 stage shift register. The shift register does not accept the word until the next positive transition of its clock $\emptyset_3$. Since the decade counter is clocked by $\overline{\emptyset}_3$, then $\emptyset_3$ goes low when $\emptyset_4$ goes high. The first $\emptyset_3$ positive transition occurs in the middle of the $\emptyset_4$ positive pulse, at T_5. In the example, the $\emptyset_4$ pulse is 1 second long. The word is jammed in 1/2 second after $\emptyset_4$ goes high. At this instant the MSB appears on the serial output of the shift register. The MSB is identified as D_8. One-half second after D_8 appears, P/S goes low. D_7 is shifted out 1 second after D_8 on the next $\emptyset_3$ transition. The next 6 bits, D_6 to D_1, appear at 1 second intervals. After D_1, S_1 and S_2 appear for 1 second each. Every tenth $\emptyset_3$ clock pulse a new word is jammed into the register. At every $\emptyset_3$ pulse a bit appears on the output. The two extra bits, S_1 and S_2, are programmable at the serial input of the shift register. Whatever is on the serial input when D_7 and D_6 are pulsed out becomes S_1 and S_2. If the "3" output from the decade counter is hardwired to the serial input, then $S_1 = 1$, $S_2 = 0$. The "4" output provides $S_1 = 0$, $S_2 = 1$. The serial input can be hardwired at 1 or 0 to make $S_1 = S_2 = 1$, or $S_1 = S_2 = 0$.

Last Word Out

12. On the negative transition of the 64th $\emptyset_4$ pulse, the Q_7 output of the read control counter goes high. This resets the Q_3, and Q_4 flip-flop outputs. $\emptyset_3$ continues to count until the "0" output on the decade counter goes high. This occurs 1/2 second after the D_1 bit appears on the serial output. The "0" output and the $\overline{Q}_3$ flip-flop are the inputs to a NAND gate. The output is inverted and connected to the reset of the $\emptyset_3$ ripple counter and the decade counter. $\emptyset_3$ is stopped and reset, the "0"

output remains high, and D_1 remains on the serial out until the next read request. At the next read request, the sequence of the first bits pulsed out will be: S_1, S_2, D_8 to D_1 of the first word, etc.

IV. OPERATING INSTRUCTIONS

The positive power input, V_{DD}, may be from 5 to 15 VDC. V_{SS} is ground, 0 VDC. V_{DD} is equivalent to logic 1 and V_{SS} is logic 0. All inputs to the memory unit operate at logic levels and must be at V_{DD} or V_{SS} when not in transition. It is not acceptable to leave an input disconnected or floating. An example is the data acquisition command input. When not in use this line must be at 0. The command is given by a rapid transition from 0 to 1. Similarly the clock inputs must be pulses between 0 and 1 with rise and fall times less than 5 usec.

Output lines may be left unattached. All outputs are digital and will be at logic 0 or 1 or in transition. All outputs have sufficient current capability to drive other CMOS circuitry. CMOS outputs can provide as much as 1 ma to drive external circuitry, but the output voltage is pulled down enough to prevent using it as input to other CMOS.

1. Connect power. Pin 1 is V_{DD} and pin 2 is V_{SS}. The memory unit will not tolerate reversed power leads.

2. Connect two-phased clock. Pins 4 and 21.

3. Connect the 8 data input leads. Pins 10 through 17.

4. See that data acquisition and data transmission input lines are at logic 0. Pins 3 and 20.

5. Connect serial input for desired coding of spacing bits. See section on serial out data. Connecting it to 0 will make both spacing bits 0. Pin 9.

6. Pin 5 is the reset and should normally be at 0. A 1 on the reset line will interrupt any read cycle and return the read control counter to 0 but will leave the address counter as it was. When turning on power, the reset should be pulsed to clear any spurious start-up activity in the memory.

7. The unit is now ready to read or write. If a read command is given, the output will consist of random numbers because the memory will not hold data after the power is turned off. Data acquisition may begin immediately, but it may be useful to set all 64 words to a known number, such as all zeros, before starting data collection.

High Speed Writing

If all data inputs are at logic 0 and the $\emptyset_2$ clock is connected to the data acquisition input, the memory will store zeros at $\emptyset_2/2$. If $\emptyset_2$ is 1 KHz, then 1 second of this high speed writing will place zeros in the memory many times over. It is advisable to hit the reset first to insure that the unit is not in a read cycle.

V. APPLICATION NOTES

1. The input impedance on all inputs is very high as typical of CMOS devices. Consequently, it is possible to hold inputs at logic 0 or 1 by pull-up or pull-down resistors tied from the inputs to V_{DD} or V_{SS}. These resistors may be on the order of 10 KΩ to 20 KΩ. Incoming digital signals will over-ride these values.

2. Figure 4 is the printed circuit layout for the board. On this figure, numbers have been added corresponding to the pins identified in Table 1. Capital letters A through L have also been added. These letters have been placed near pin 1 of the CMOS package they identify. The CMOS type is given in Table 2.

TABLE 2

CMOS PACKAGE IDENTIFICATION

A. Solid State Scientific SCL5555D Random Access 64 X 4 Memory

B. CD4004AE 7 Stage Ripple Counter "Address Counter"

C. SCL5555D 64 X 4 Memory

D. CD4014AE 8 Stage Static Shift Register

E. CD4017AE Decade Counter

F. CD4020AE or CD4040AE 12 or 14 Stage Ripple Counter, "ϕ_3 clock." The CD4020AE and CD4040AE are interchangeable.

G. CD4004AE "Read Control Counter"

H. CD4011AE Quad 2-input NAND Gate

I. CD4001AE Quad 2-input NOR Gate

J. CD4013AE Dual D Flip-Flop

K. CD4001AE Quad 2-input NOR Gate

L. CD4013AE Dual D Flip-Flop

All packages, except A and C, are RCA COS/MOS Digital Integrated Circuits. Further information may be obtained from the RCA Solid State Databook Series, volume SSD-203A, which is available free from RCA. Data sheets on the random access memory is available on request from Solid State Scientific.

3. Figure 5 shows a simple CMOS circuit that converts the serial output to high and low tones, corresponding to 1's and 0's. This circuit also inhibits this tone generation during the S_2 spacing bit, thus creating a silent space between words.

The serial out line is connected to the tone generating astable multivibrators through control gates. When the serial out is 0, the low tone astable turns on; and when the serial out is 1, the high tone astable operates. The output from both astables is gated through a 3 input NAND gate. The third NAND input comes from a monostable that is triggered by the ϕ_3 clock. The ϕ_3 clock has been gated through a NOR gate by the "1" decade output. When "1" is high, the ϕ_3 clock is inhibited. This occurs only during the ϕ_3 positive transition that pulses out the S_2 bit.

The output from the 3 input NAND gate is a series of tone bursts. Each burst begins on the positive transition of the ϕ_3 clock. Each burst lasts ∿80 ms. The serial out information is S_1, space, D_8, D_7, $D_6 \ldots D_1$, S1, space D_8, etc. The amplified output from this circuit may go directly to a speaker or an acoustic transmitter.

4. Figure 6 shows a CMOS circuit that generates the two-phased clock pulses that are necessary for operation of the memory unit. This clock circuit is the one that was used in the test model of the memory unit. It generates the ϕ_1 and ϕ_2 clock pulses that are shown on the timing diagram. The circuit consists of an astable multivibrator that has a 1 KHz square wave output which is ϕ_1. ϕ_1 is attached to the ϕ_1 input to the memory and also to a D type flip-flop, as shown in Figure 6. This flip-flop provides the delay between the ϕ_1 and ϕ_2 pulses. The second flip-flop regulates the length of the ϕ_2 pulse. Grounds are shown as logic zeros and positive voltage connections as ones.

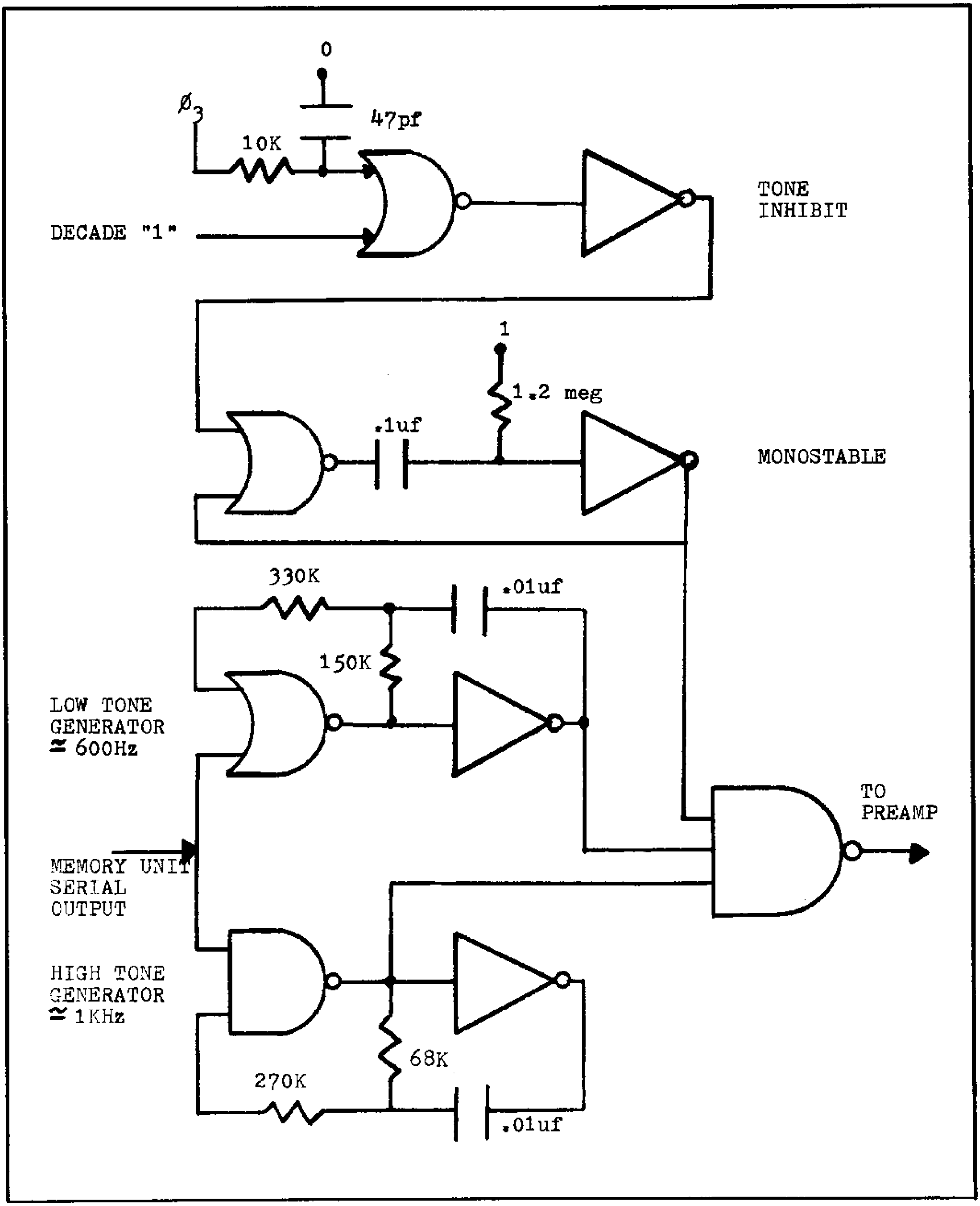

Figure 5. Digital Tone Generator

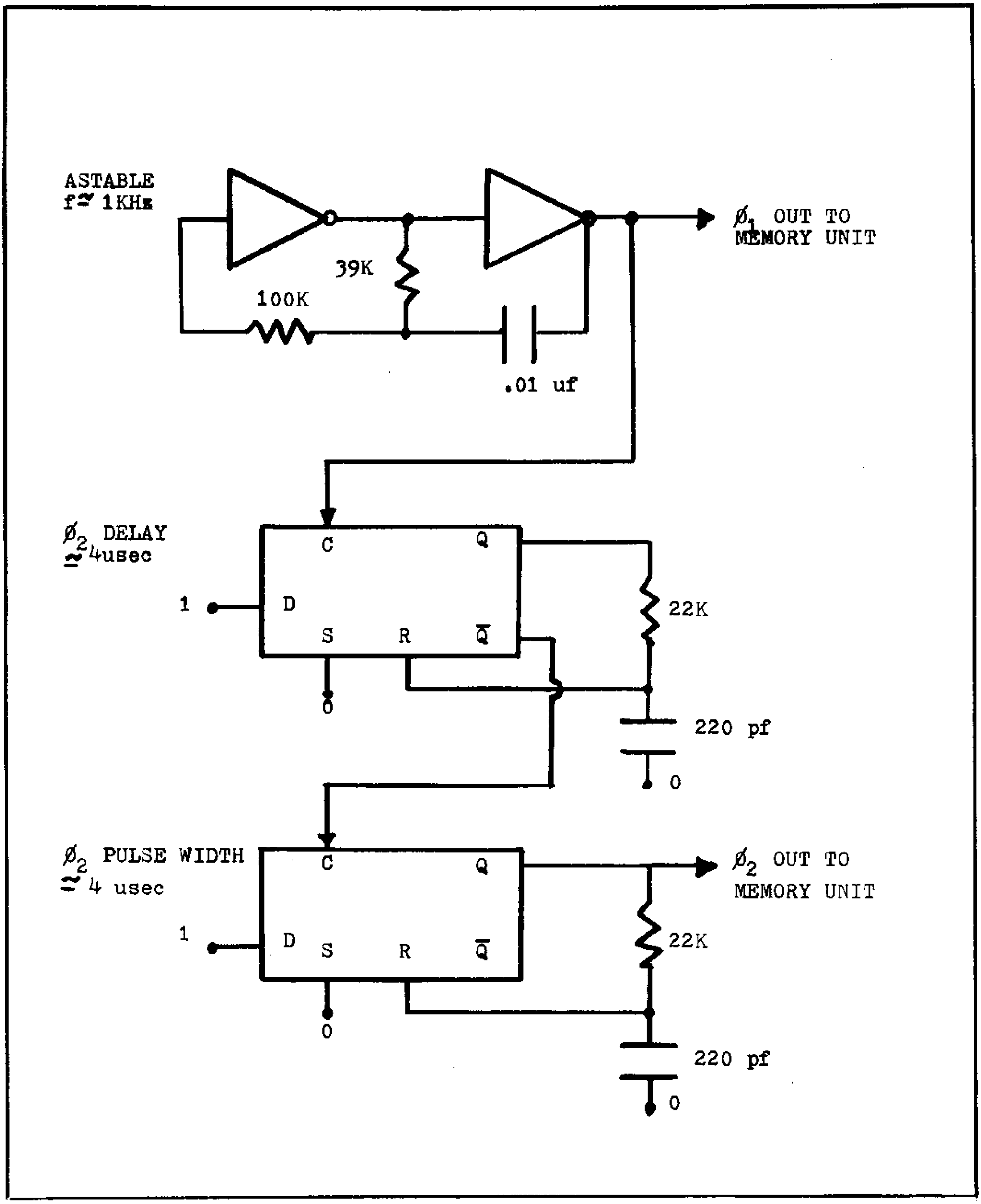

Figure 6. Clock Logic Circuit

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